

Crystal Clock Oscillator

- 50 pf load capable
- 3.3 VDC input available
- TTL and CMOS compatible
- Optional tristate

Series **CH11**



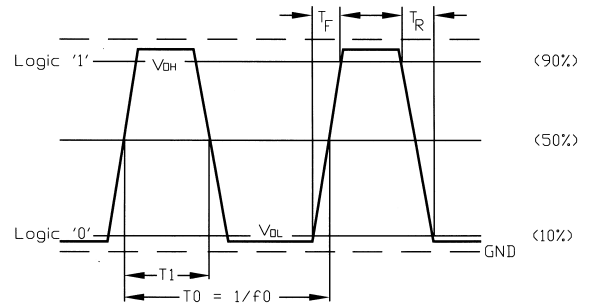
Part Numbering Example: CH11 00 4 L 45 - A2 - 50.0 TS

CH11	00	4	L	45	A2	50.0	TS
SERIES	STABILITY	PACKAGE STYLE	VOLTAGE	SYMMETRY	OPERATING TEMP.	FREQUENCY	
CH11	00 = ±100 ppm 50 = ± 50 ppm 25 = ± 25 ppm 10 = ± 10 ppm	1 = Full Size 3 = Full Size, Gull Wing 4 = Half Size 6 = Half Size, Gull Wing	Blank = 5V L = 3.3V	Blank = 40/60% 45 = 45/55%	Blank = 0°C ~ +70°C A2 = -40°C ~ +85°C		Blank = No Connection TS = Tristate, pin 1

Specifications:

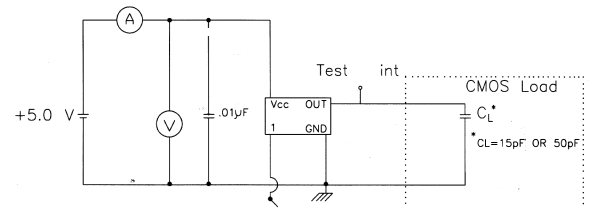
Frequency Range:	1.8432 MHz to 100.000 MHz
Available Stability Options:	±100 ppm <i>Standard</i> ±50 ppm ±25 ppm ±10 ppm
Output Series:	TTL/CMOS
Input Voltage:	+5.0 VDC ±10% <i>Standard</i> +3.3 VDC ±10%
Operating Temperature Range Options:	-10°C to +70°C <i>Standard</i> -40°C to +85°C
Output Voltage:	HCMOS V _{OL} = 10% V _{DD} V Max. HCMOS V _{OH} = 90% V _{DD} V Min.
Output Load:	10 TTL, 50 pf CMOS
Maximum Input Current:	25 mA (1.8432 to 24.999 MHz) 45 mA (25.000 to 49.999 MHz) 70 mA (50.000 to 69.999 MHz) 80 mA (70.000 to 100.000 MHz)
Maximum Rise/Fall Time:	7 ns
Duty Cycle:	40/60% <i>Standard</i> 45/55%
Max. Start-Up Time:	10 ms
Tristate Input:	@+5 VDC Input +0.80 VDC Max. to Disable +3.60 VDC Min. to Enable or Open to Enable @+3.3 VDC Input +0.80 VDC Max. to Disable +2.20 VDC Min. to Enable or open to Enable
Storage Temperature:	-55°C to +125°C

OUTPUT WAVE FORM



$$\text{SYMMETRY} = \left(\frac{T_1}{T_0} \right) \times 100\%$$

TEST CIRCUIT



* Includes stray and probe capacitance (15pF TYP)

