SERIES	CJTDAE CJTDAL

The Cardinal Cappuccino Crystal Oscillator LVDS/ LVPECL TCXO

Features

- 3.3V supply voltage- configurable
- 10MHz to 250MHz LVDS and LVPECL outputs- configurable
- Better than 2Hz tuning resolution
- Low power, typically 23mA LVDS and 54mA LVPECL
- Temperature range: -30°C to +75°C
- Stability: ± 2.5ppm
- Phase Jitter (12kHz – 20MHz)
- Switches between 2 Frequencies

Applications

- Multimedia
- Computing
- Networking, etc.

Part Numbering Example: CJTDA E 7 L Z - A3 B3 - XXX.XXX / YYY.YYY TS

CJTDA	E	7	L	Z	A3	B3	XXX.XXX	YYY.YYY
SERIES	OUTPUT	PACKAGE STYLE	VOLTAGE	ADDED FEATURES	OPERATING TEMP.	STABILITY	FREQ. 0	FREQ. 1
CJTDA	L = LVDS E = LVPECL	7 = 7 X 5 .	L = 3.3V	Z = Tape and Reel	A3 = -30°C to +75°C	B3 = ± 2.5ppm	10-250MHz PIN 2 Logic "0"	10-250MHz PIN 2 Logic "1"

*TS = Tristate

Specification

Waveform	LVDS/ LVPECL
Frequency	10MHz to 250MHz
Operating Temperature Range	-30°C to +75°C
Storage Temperature Range	-40°C to +85°C
Supply Voltage	3.3V
Frequency Stability vs. Temp. Range	±2.5ppm
Input Current	23/54mA
Phase Jitter (12kHz to 20MHz):	0.4ps to 1.5ps rms max
Start-Up Time	10ms Max
Enable/ Disable Input Voltage	VIH ≥ 0.7VDD or No Connection, VIL ≤ 0.3VDD or Ground
Aging/ Year	±3ppm Max

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Description

The Cardinal Cappuccino crystal oscillator is based on a high performance integrated circuit designed for use in Cardinal's continued expanding leadership products in the programmable frequency control industry. Cardinal's new Cappuccino design is today state of the art in oscillators. The Cappuccino line product features 10MHz to 1.5GHz with CJTDAE/ CJTDAL ranging 10MHz to 250MHz Output, 3.3V Supply Voltage, LVDS/ LVPECL commercial -20°C to +70ºC and industrial temperature range -30°C to +75ºC.

Cardinal's new CJTDAE/ CJTDAL series is competitively priced and has the lowest typical power consumption 23/54mA LVDS/ LVPECL (70% less power than the Fox XpressO™ oscillator), lowest jitter and best phase noise over 12kHz to 20MHz vs. the traditional fixed frequency quartz oscillators and Surface Acoustic Wave oscillators. Cardinal's programming centers utilize modern robotics, for testing, programming and 100% final testing as we do with all our programmable offerings. The Cardinal CJTDAE/ CJTDAL series line is offered in both ceramic and low cost plastic industry standard packages.

Cardinal's Cappuccino line fits in all applications requiring a reference frequency including Multimedia, Computing, Networking, consumer etc.

Absolute Maximum Ratings

Item	Symbol	Condition	Unit
Input Voltage	V_I	-0.5 to V_{DD} + 0.5	V
Output Voltage	V_O	-0.5 to V_{DD} + 0.5	V
Positive Supply Voltage	V_{DD}	4.2	V
Storage Temperature		-40 to +85	°C

DC Electric Characteristics (T = 25°C)

Unless stated otherwise, the data presented here was taken over the following parameters, V_{DD} = 3.3V ± 10%, Ta = -30°C to +75°C (industrial)

Item		Symbol	Specification			
			Min	Typ	Max	Units
Power Supply (V_{DD}, GND pins)	Power Supply Voltage	V_{DD}	2.97	3.3	3.63	V
	LVDS I_{DD}	I_{DD}		23		mA
	LVPECL I_{DD}	I_{DD}		54		mA
	Current w/Output Disabled	I_{OED}		16		mA
	Rise Time	V_{DD}	100			µS

Item		Symbol	Specification			
			Min	Typ	Max	Units
AC Characteristics						
Outputs						
LVDS (OUT, nOUT)	Frequency Range	F_{LVDS}	10		250	MHz
	Stability		-2.5		+2.5	ppm
	Operating Temperature		-30		+75	°C
	Differential Output Voltage	V_{OD}	175	350		mV
	V_{OD} Magnitude Change	Δ_{VOD}			50	mV
	Offset Voltage	V_{OS}		1.25		V
	V_{OS} Magnitude	ΔV_{OS}			50	mV
	Duty Cycle	$DODC_{LVDS}$	45		55	%
	Rise Time	t_R	125		350	ps
	Fall Time	t_F	150		350	ps
LVPECL (OUT, nOUT)	Frequency Range	F_{LVPECL}	10		250	MHz
	Stability		-2.5		+2.5	ppm
	Operating Temperature		-30		+75	°C
	Output High Voltage	V_{OH}	V_{DD} - 1.03		V_{DD} - .6	V
	Output Low Voltage	V_{OL}	V_{DD} - 1.85		V_{DD} - 1.6	V
	Differential Duty Cycle	$DODC_{LVPECL}$	45		55	%
	Rise Time	t_R	150		250	ps
	Fall Time	t_F	150		250	ps
OE Turn On Time (<50MHz)		$OE_{LOW/HIGH}$			200	ns
OE Turn On Time (>50MHz)		$OE_{LOW/HIGH}$			100	ns
OE Turn Off Time		$OE_{HIGH/LOW}$			50	ns
Jitter	Phase Jitter (12kHz to 20MHz)	tjit	0.4	0.9	1.5	ps rms
	Period Jitter	$t_{RMS, DIFF}$		3	4.5	ps
		$t_{p-p, DIFF}$		30	45	ps

Performance Characteristic Curves

Unless otherwise specified, data is characterized over temperature range -30°C to +75°C and voltage range 2.97V - 3.63V.

I_{DD} vs. V_{DD}

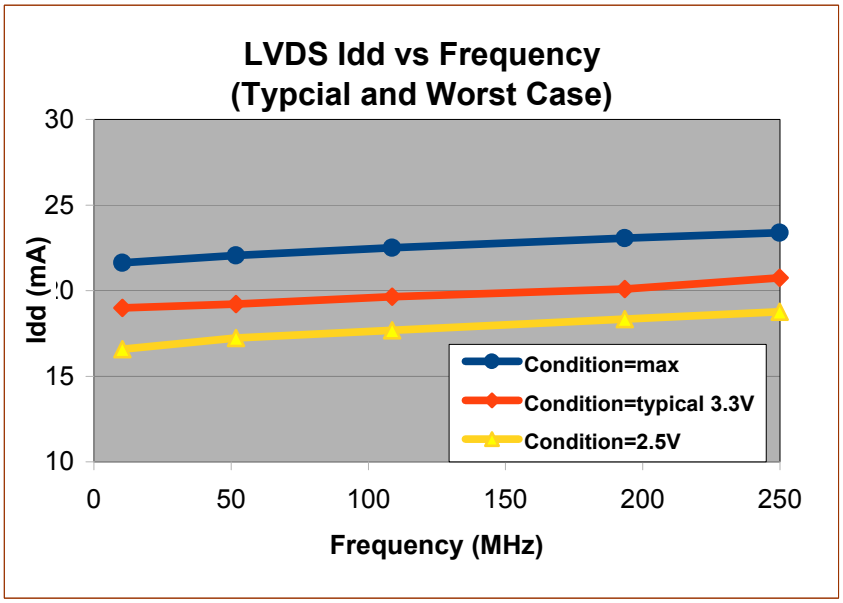


Figure 1. LVDS I_{DD} vs. Frequency, V_{DD}.

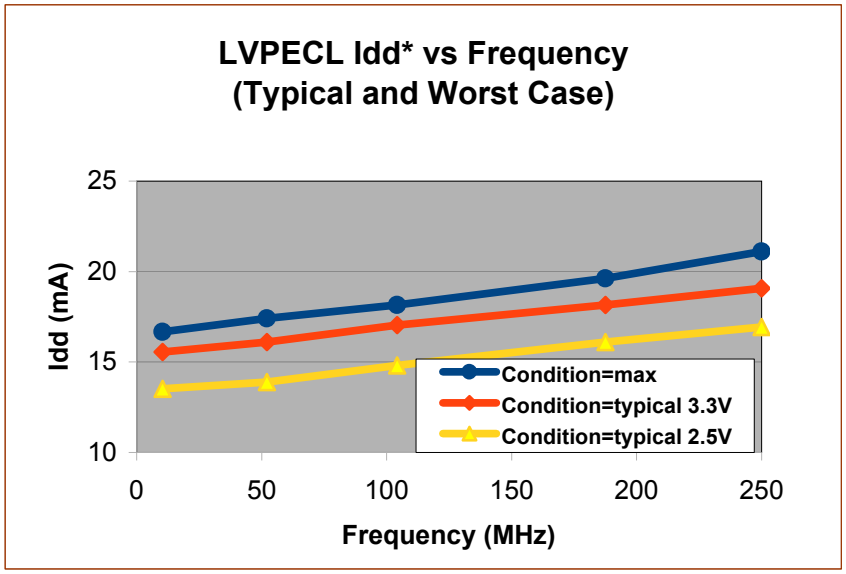


Figure 2. LVPECL I_{DD} vs. Frequency, V_{DD}

***Note: LVPECL Idd does not include output load current**
Add 32 mA to incluce outpute load current

OE Turn-on and Turn-off Times

Notes:

- These measurements were all performed with an AC coupled output so that leakage currents do not affect the timing of the measurement. This results in all outputs floating to the midpoint of the signal levels when off.
- When LVDS is disabled the output goes to the common mode voltage (approximately 1.25V).
- When LVPECL is disabled the output goes to tri-state level which floats to Vol.

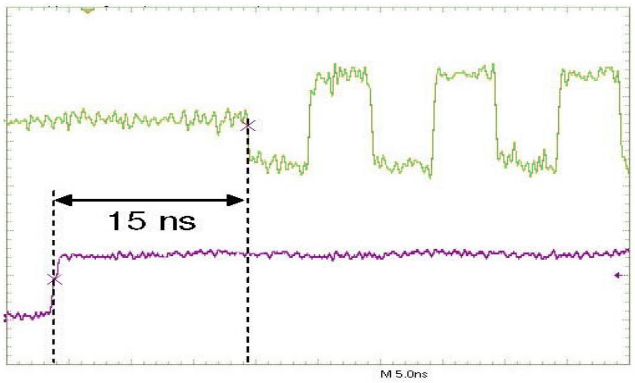


Figure 5. 3.3V LVDS OE Enabled Time

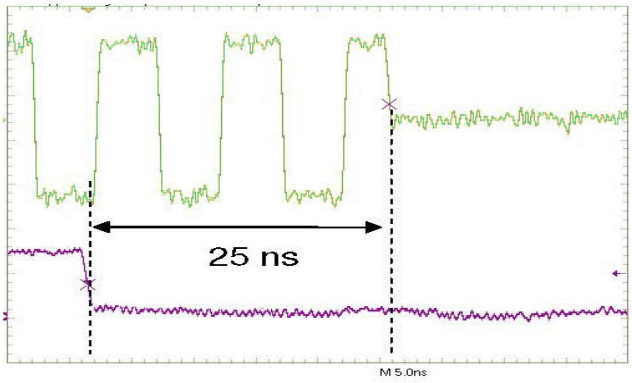


Figure 6. 3.3V LVDS OE Disabled Time

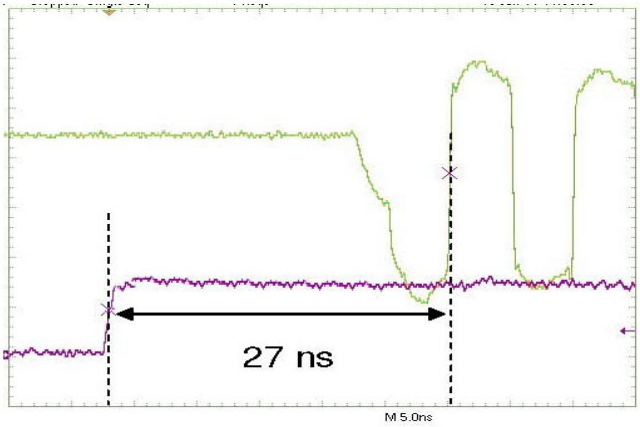


Figure 7. 3.3V LVPECL OE Enabled Time

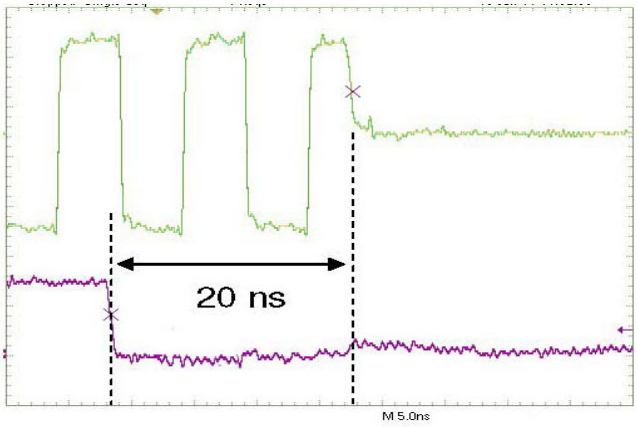


Figure 8. 3.3V LVPECL OE Disabled Time

Waveform Measurements

The following figures are descriptions for how the waveforms are measured for the datasheet applications.

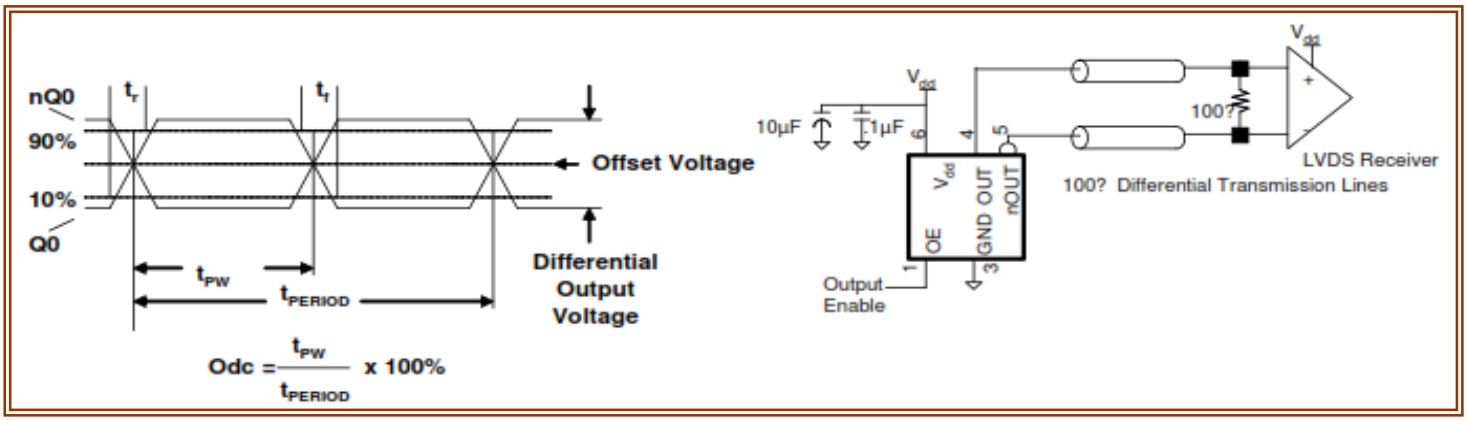


Figure 11. 3.3V LVDS waveform measurement test setup

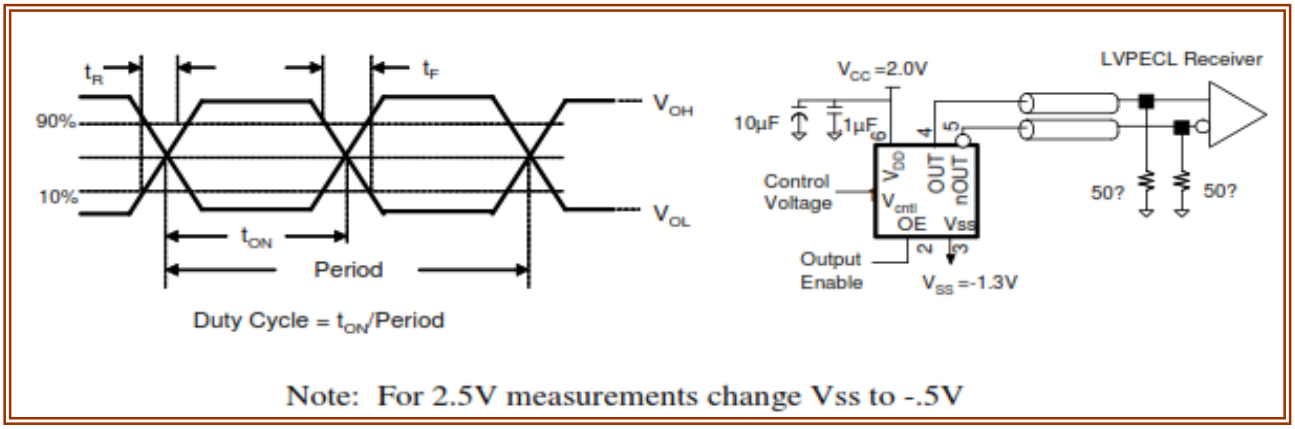


Figure 12. 3.3V LVPECL waveform measurement test setup

Application Information

Termination for 3.3V LVPECL Output

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts offered are recommended only as guidelines.

OUT and nOUT are low impedance following outputs that generate LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figures 13 and 14 present two different designs. They are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designer simulate to guarantee compatibility across all printed circuit and clock component process variations.

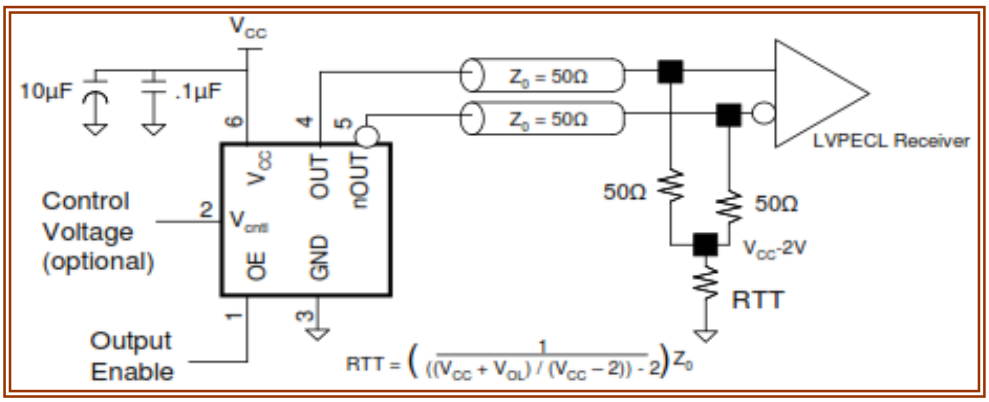


Figure 13. 3.3V LVPECL XO Application Schematic & Power Supply Decoupling

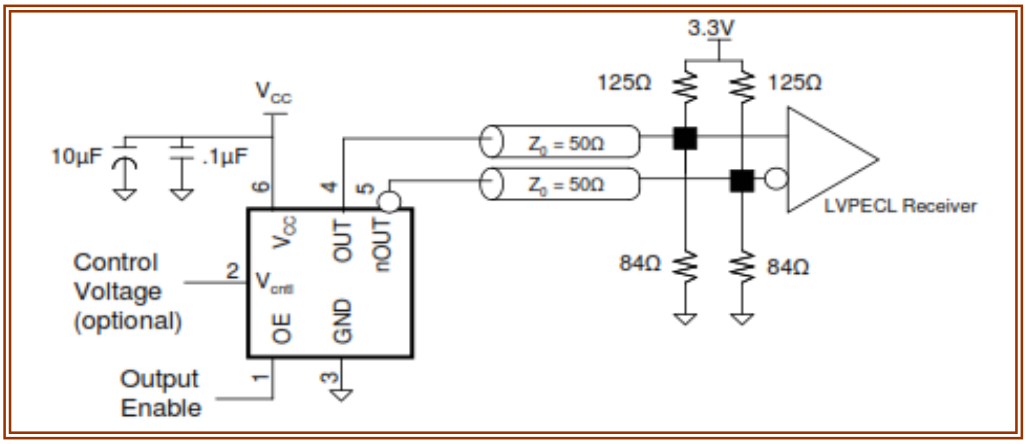


Figure 14. Alternante 3.3V LVPECL XO Application Schematic & Power Supply Decoupling

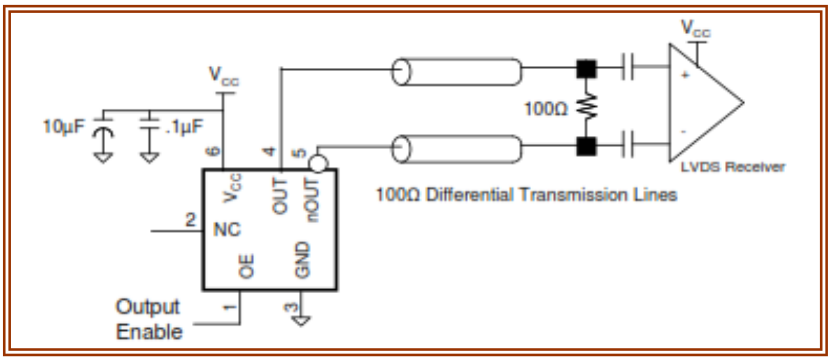


Figure 18. Termination for 3.3V LVDS Output

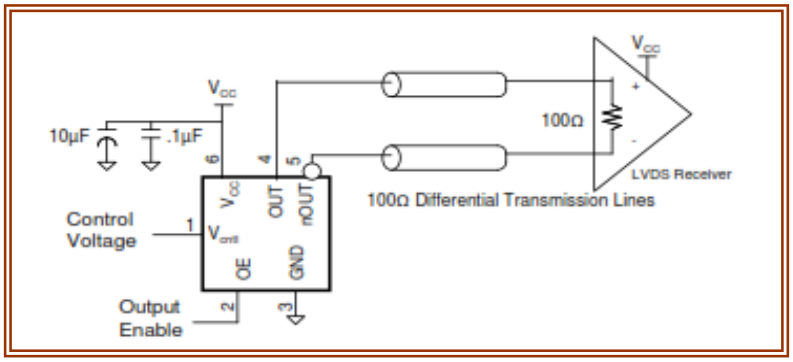
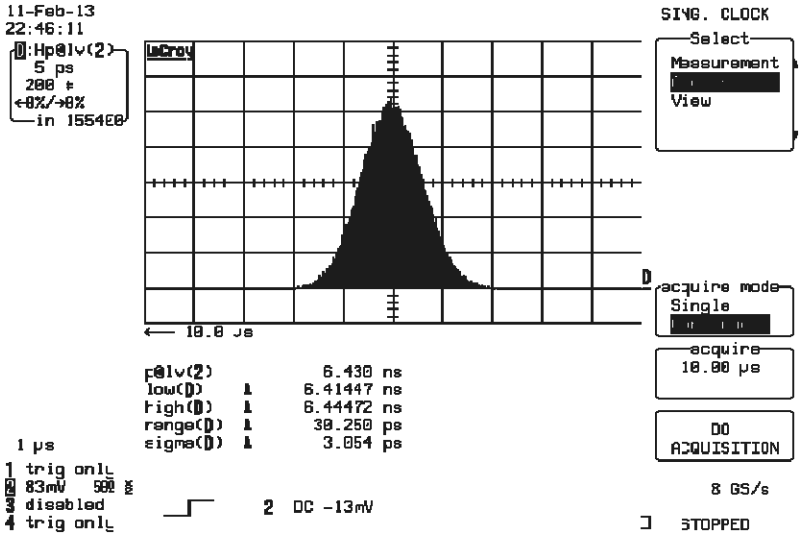
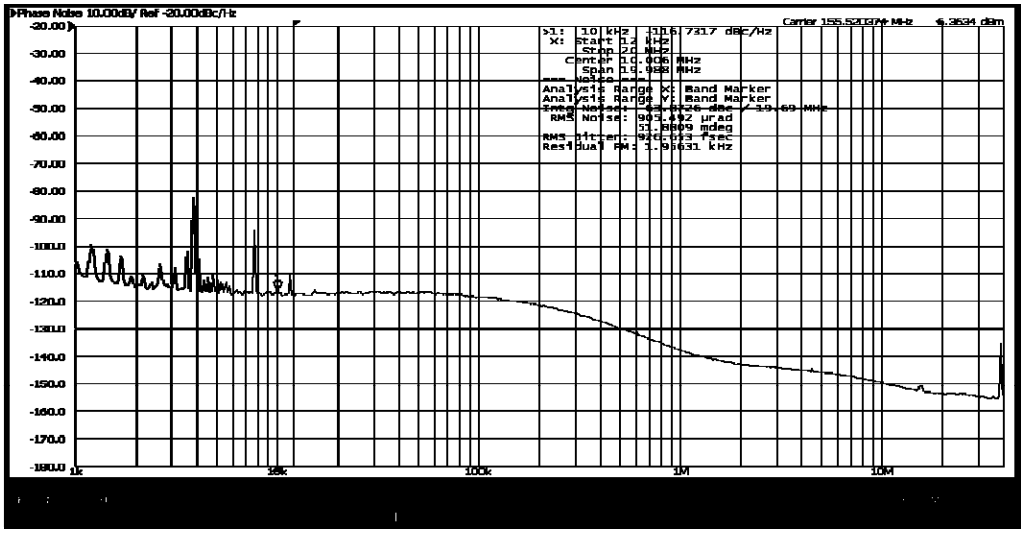
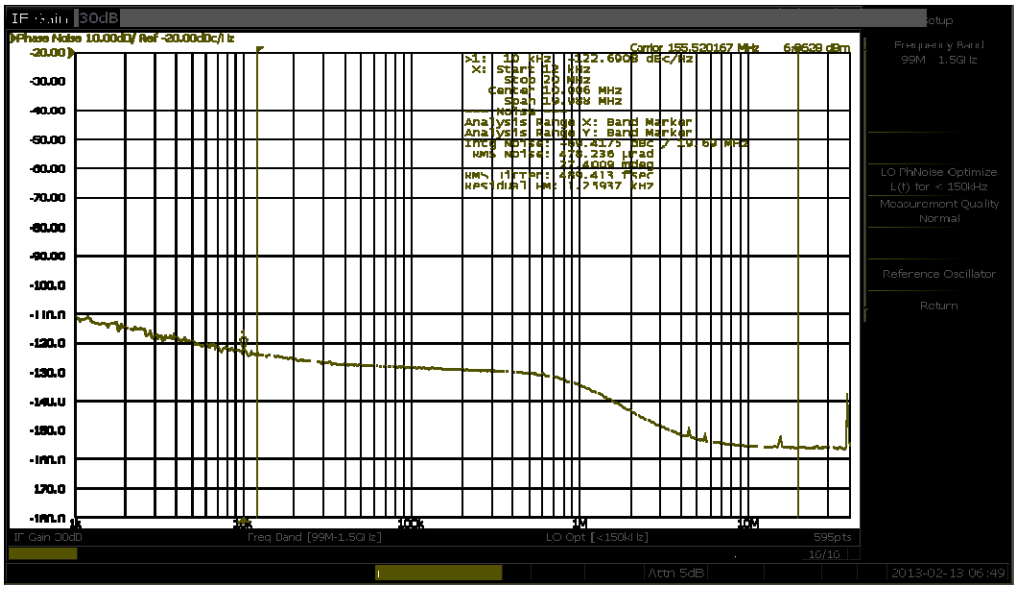


Figure 19. 3.3V LVDS XO Application Schematic & Power Supply Decoupling

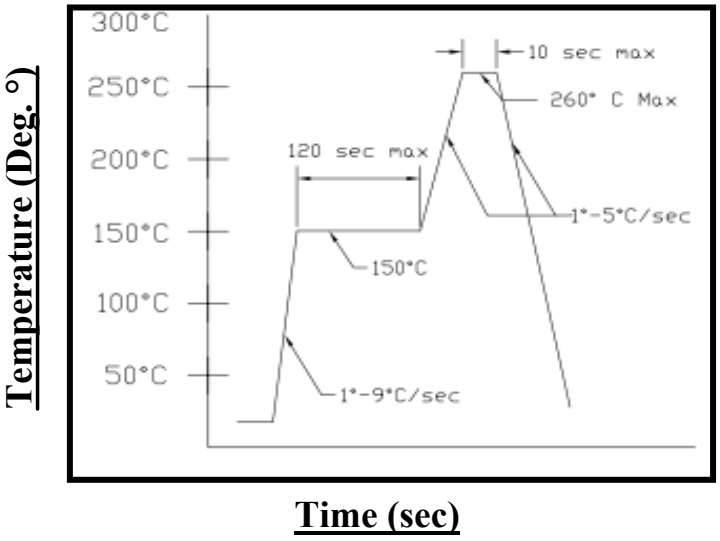
Phase Noise & Jitter Plots







Recommended Solder Profile for
Cardinal Components, Inc.
Package Infared Reflow.
Do Not Use Ultrasonic-Wave Soldering or
Wave Solder with Package Immersed in Solder
Damage to Crystal will result.



Reliability

Cardinal Components Inc., qualification includes aging at various extreme temperatures, shocks and vibration, temperature cycling, and IR reflow simulation. The Cappuccino family meets the following qualification tests:

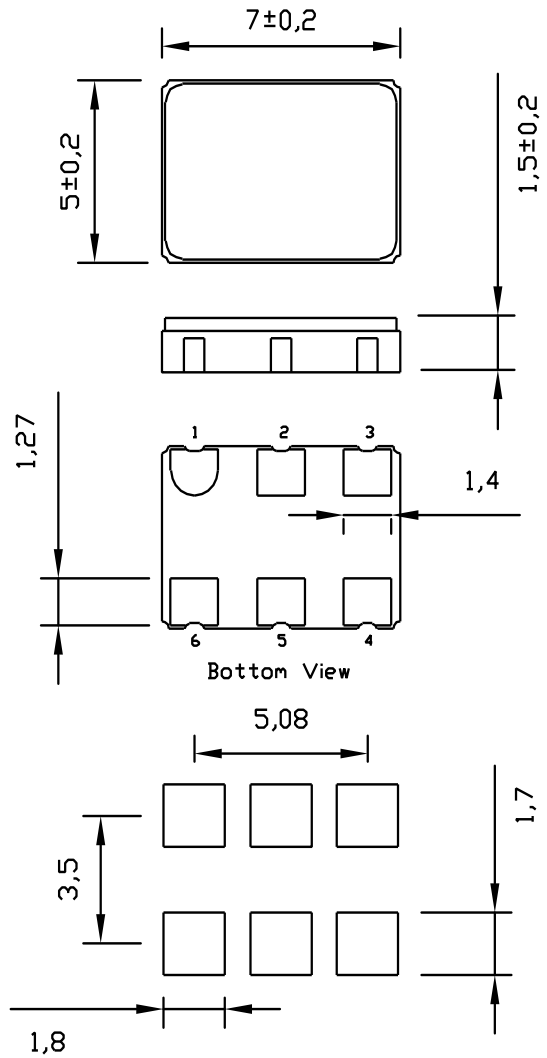
Environmental Compliance	
Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016
Moisture Sensitivity Level	IPC/ JEDEC J-STD-020, MSL1

Handling Precautions

Although ESD protection circuitry has been designed into the Cappuccino proper precautions should be taken when handling and mounting. Cardinal employs a human body model (HBM) and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation.

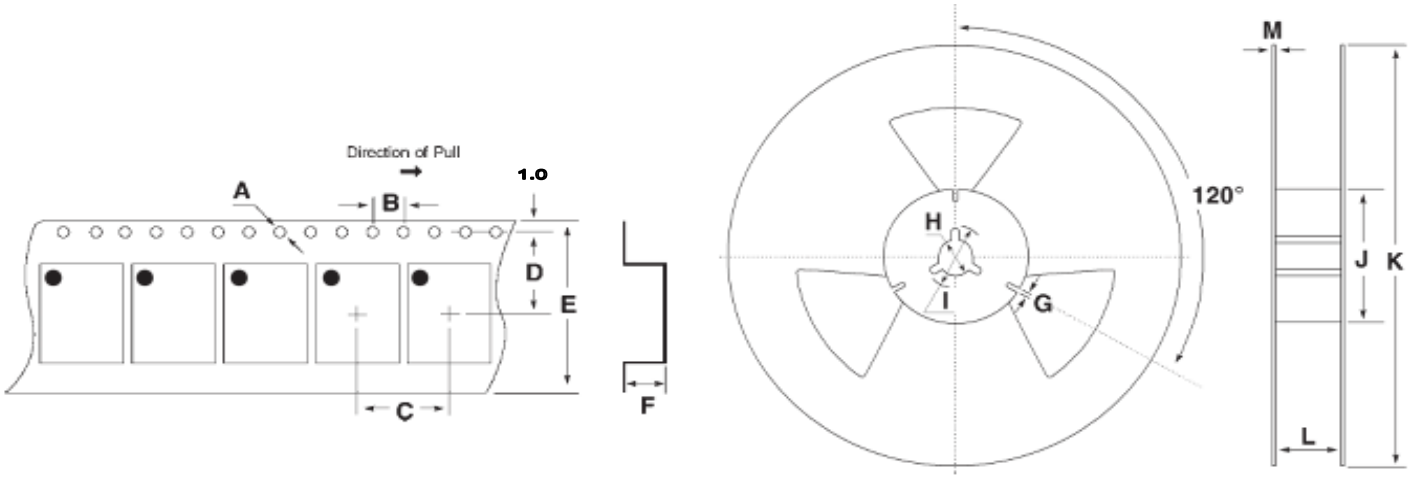
ESD Ratings		
Model	Minimum	Conditions
Human Body Model	1000V	MIL-STD-883, Method 3015
Charged Device Model	900V	JEDEC, JESD22-C101
Machine Model	200V	JEDEC, JESD22-A115-A

Style 7: 5x7mm



6 Pad LVDS/ LVPECL	
Pin 1	OE
Pin 2	FS Frequency Select
Pin 3	GND
Pin 4	Out
Pin 5	nOUT
Pin 6	V_{DD}

Tape and Reel Specifications



Tape Specifications (mm)							
Package	A	B	C	D	E	F	QTY
7 = 7 X 5	1.5	4.0	8.0	7.5	16.0	2.2	1,000

Reel Specifications (mm)							
Package	G	H	I	J	K	L	M
7 = 7 X 5	2.0	13	21	60	180	17.0	1.25