



The Cardinal Cappuccino Crystal Oscillator LVDS/ LVPECL VCXO

Features

- 2.5V or 3.3V supply voltage- configurable
- 750MHz to 1500MHz LVDS and LVPECL outputs- configurable
- Better than 2Hz tuning resolution
- Low power, typically 23mA LVDS and 54mA LVPECL
- Temperature range: -40°C to +85°C
- Stability: ± 25ppm
- APR: ± 50ppm
- Phase Jitter (12kHz – 20MHz) .9ps RMS

Applications

- Multimedia
- Computing
- Networking, etc.

Part Numbering Example: CJVY E 7 L Z - A7 BR - XXX.XXX TS

CJVY	E	7	L	Z	A7	BR	XXX.XXX	TS
SERIES	OUTPUT	PACKAGE STYLE	VOLTAGE	ADDED FEATURES	OPERATING TEMP.	STABILITY	FREQUENCY	TRI-STATE
CJVY	L = LVDS	2 = 2.5 X 2	S = 2.5V	Z = Tape and Reel	A7 = -40°C to +75°C	BR = ± 25ppm		
	E = LVPECL	5 = 5 X 3.2		L = 3.3V		BP = ± 50ppm		
		7 = 7 X 5 .						TS = Tri-State

Specification

Waveform	VCXO LVDS/ LVPECL
Frequency	750MHz to 1500MHz
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Supply Voltage	2.5V, 3.3V
Frequency Stability vs. Temp. Range	±25ppm/ ±50ppm
Input Current	23/54mA
Phase Jitter	.9ps Typical
Start-Up Time	10ms Max
Enable/ Disable Input Voltage	VIH ≥ 0.7VDD or No Connection, VIL ≤ 0.3VDD or Ground
Aging/ Year	±3ppm Max

Description

The Cardinal Cappuccino crystal oscillator is based on a high performance integrated circuit designed for use in Cardinal's continued expanding leadership products in the programmable frequency control industry. Cardinal's new Cappuccino design is today state of the art in oscillators. The Cappuccino line product features 10MHz to 1.5GHz with CJVYE/ CJVYL ranging 750MHz to 1500MHz Output, 2.5V or 3.3V Supply Voltage, VCXO LVDS/ LVPECL commercial -20°C to +70°C and industrial temperature range -40°C to +85°C.

Cardinal's new CJVYE/ CJVYL series is competitively priced and has the lowest typical power consumption VCXO LVDS/ LVPECL (70% less power than the Fox XpressO™ oscillator), lowest jitter and best phase noise over 12 kHz to 20 MHz vs. the traditional fixed frequency quartz oscillators and Surface Acoustic Wave oscillators. Cardinal's programming centers utilize modern robotics, for testing, programming and 100% final testing as we do with all our programmable offerings.

Cardinal's Cappuccino line fits in all applications requiring a reference frequency including Multimedia, Computing, Networking, hand held, consumer etc.

Absolute Maximum Ratings

Item	Symbol	Condition	Unit
Input Voltage	V _I	-0.5 to V _{DD} + 0.5	V
Output Voltage	V _O	-0.5 to V _{DD} + 0.5	V
Positive Supply Voltage	V _{DD}	4.2	V
Storage Temperature		-55 to +125	°C

DC Electric Characteristics (T = 25°C)

Unless stated otherwise, the data presented here was taken over the following parameters, $V_{DD} = 3.3V \pm 10\%$ or $2.5V \pm 5\%$, $T_a = -40^\circ C$ to $+85^\circ C$ (industrial)

Item	Symbol	Specification			
		Min	Typ	Max	Units
Power Supply (V_{DD} , GND pins)	V_{DD}	2.97	3.3	3.63	V
	V_{DD}	2.375	2.5	2.625	V
	I_{DD}		23		mA
	I_{DD}		54		mA
	I_{OED}		16		mA
Rise Time	T_{VDD}	100			μs
Vc pin	Input High Voltage ($V_{DD} = 3.3V$)	V_{IH}		$V_{DD} + .1*V_{DD}$	V
	Absolute max Voltage ($V_{DD} = 3.3V$)			4	V
	Input High Voltage ($V_{DD} = 2.5V$)			$V_{DD} + .05*V_{DD}$	V
	Input Low Voltage	V_{IL}	-0.3		V
	Input High Current	I_{IH}		5	μA
	Input Low Current	I_{IL}	-5		μA
	Input Impedance			1	MΩ
	Vc Bandwidth		10		kHz
Output Enable OE Pin Input	Vc Pull		-100		100 ppm
	Input High Voltage	V_{IH}	$0.7 * V_{DD}$		V
	Input Low Voltage	V_{IL}		$0.3 * V_{DD}$	V
	Input High Current	I_{IH}		5	μA
	Input Low Current	I_{IL}	-10		μA
LVCMS/ LVTTL	Equivalent Internal Pullup Resistance	R_{PULLUP}		900	κΩ

CARDINAL COMPONENTS, INC.

CJVYE/ CJVYL 750MHz - 1500MHz

Item	Symbol	Specification			
		Min	Typ	Max	Units
AC Characteristics					
Outputs					
LVDS (OUT, nOUT)	Frequency Range	F _{LVDS}	750	1500	MHz
	Stability		-25	+25	ppm
	Operating Temperature		-40	+85	°C
	Differential Output Voltage	V _{OD}	175	350	mV
	V _{OD} Magnitude Change	ΔV _{OD}		50	mV
	Offset Voltage	V _{OS}		1.25	V
	V _{OS} Magnitude	ΔV _{OS}		50	mV
	Duty Cycle	DODC _{LVDS}	45	55	%
	Rise Time	t _R	125	350	ps
LVPECL (OUT, nOUT)	Fall Time	t _F	150	350	ps
	Frequency Range	F _{LVPECL}	750	1500	MHz
	Stability		-25	+25	ppm
	Operating Temperature		-40	+85	°C
	Output High Voltage	V _{OH}	V _{DD} - 1.03	V _{DD} - .6	V
	Output Low Voltage	V _{OL}	V _{DD} - 1.85	V _{DD} - 1.6	V
OE Turn On Time (<50MHz)	Differential Duty Cycle	DODC _{LVPECL}	45	55	%
	Rise Time	t _R	150	250	ps
	Fall Time	t _F	150	250	ps
	OE Turn On Time (>50MHz)	OE _{LOW/HIGH}		200	ns
OE Turn Off Time		OE _{LOW/HIGH}		100	ns
Jitter	Phase Jitter (12kHz to 20MHz)	t _{jit}	0.4	0.9	1.5 ps rms
	Period Jitter	t _{RMS, DIFF}		3	4.5 ps
		t _{p-p, DIFF}		30	45 ps



145 Route 46 West
Wayne, NJ 07470

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Tel: (973)785-1333
E-Mail: sales@cardinalxtal.com
Web: www.cardinalxtal.com
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Performance Characteristic Curves

Unless otherwise specified, data is characterized over temperature range -40°C to +85°C and voltage range 2.2V - 3.63V.

I_{DD} vs. V_{DD}

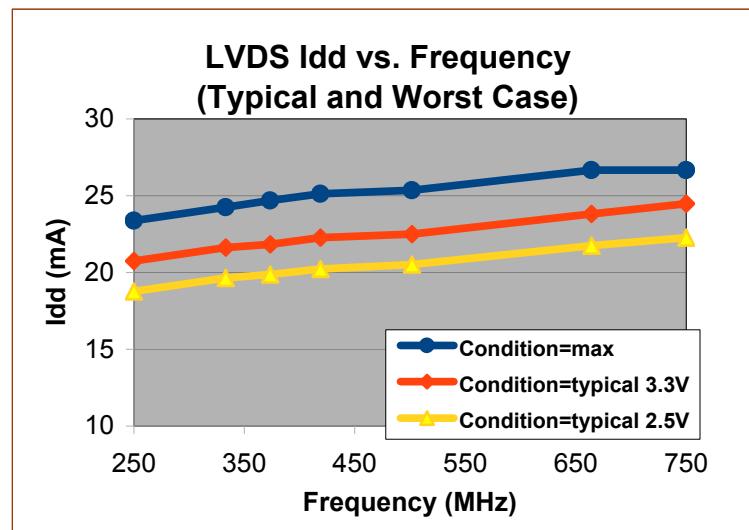


Figure 1. LVDS I_{DD} vs. Frequency, V_{DD}

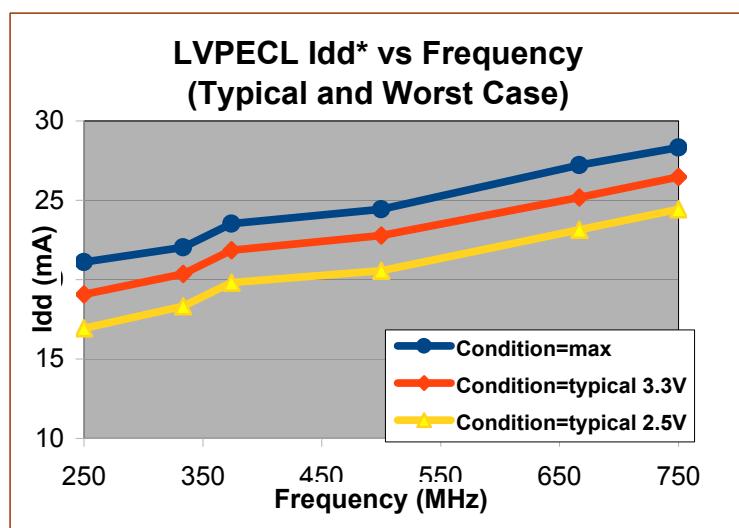


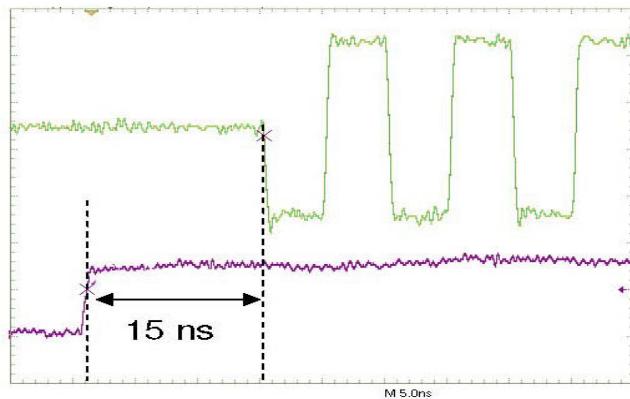
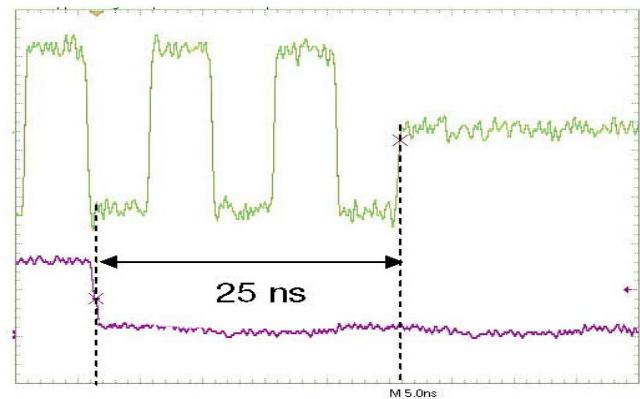
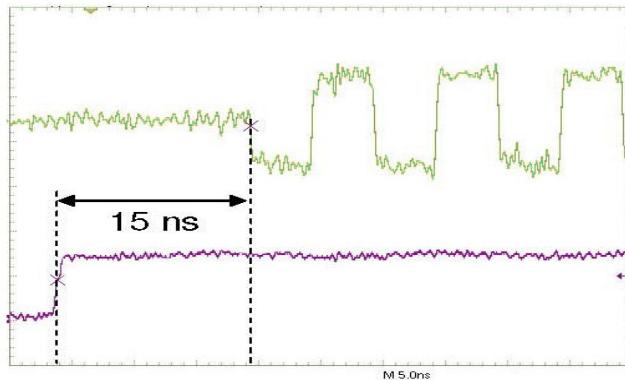
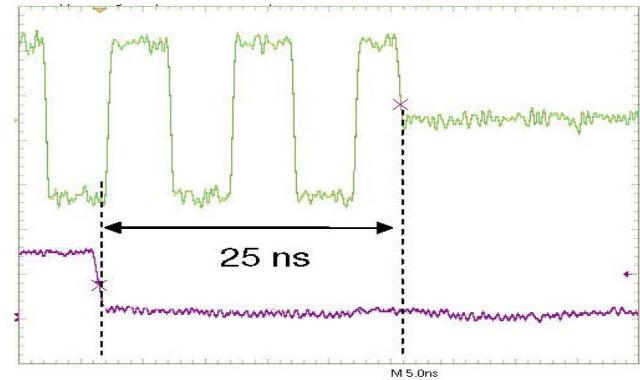
Figure 2. LVPECL I_{DD} vs. Frequency, V_{DD}

*Note: LVPECL I_{DD} does not include output load current
Add 32 mA to include output load current

OE Turn-on and Turn-off Times

Notes:

- These measurements were all performed with an AC coupled output so that leakage currents do not affect the timing of the measurement. This results in all outputs floating to the midpoint of the signal levels when off.
- When LVDS is disabled the output goes to the common mode voltage (approximately 1.25V).
- When LVPECL is disabled the output goes to tri-state level which floats to V_{OL} .

**Figure 3.** 2.5V LVDS OE Enabled Time**Figure 4.** 2.5V LVDS OE Disabled Time**Figure 5.** 3.3V LVDS OE Enabled Time**Figure 6.** 3.3V LVDS OE Disabled Time

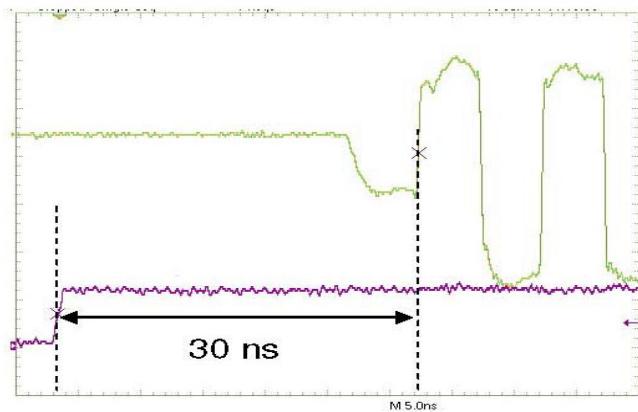


Figure 7. 2.5V LVPECL OE Enabled Time

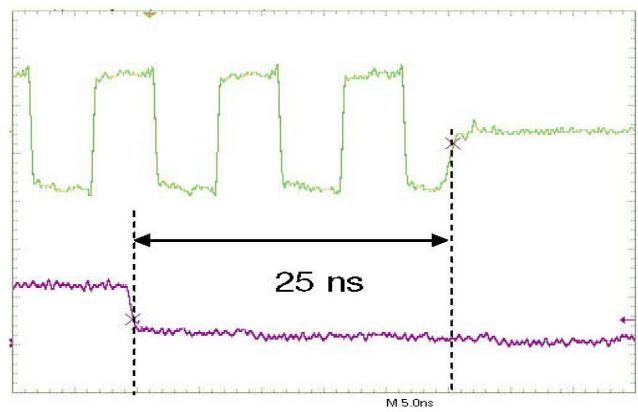


Figure 8. 2.5V LVPECL OE Disabled Time

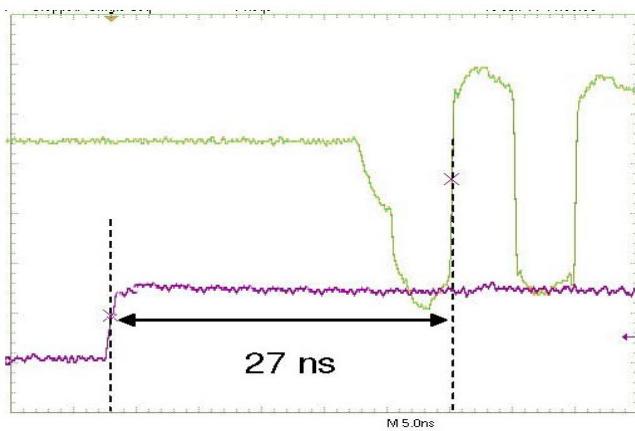


Figure 9. 3.3V LVPECL OE Enabled Time

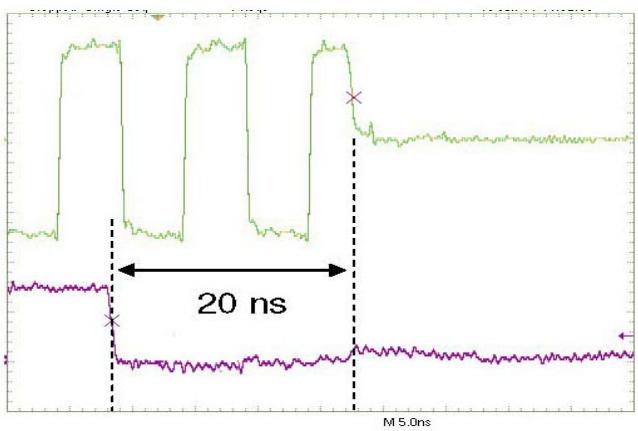


Figure 10. 3.3V LVPECL OE Disabled Time

Waveform Measurements

The following figures are descriptions for how the waveforms are measured for the datasheet applications.

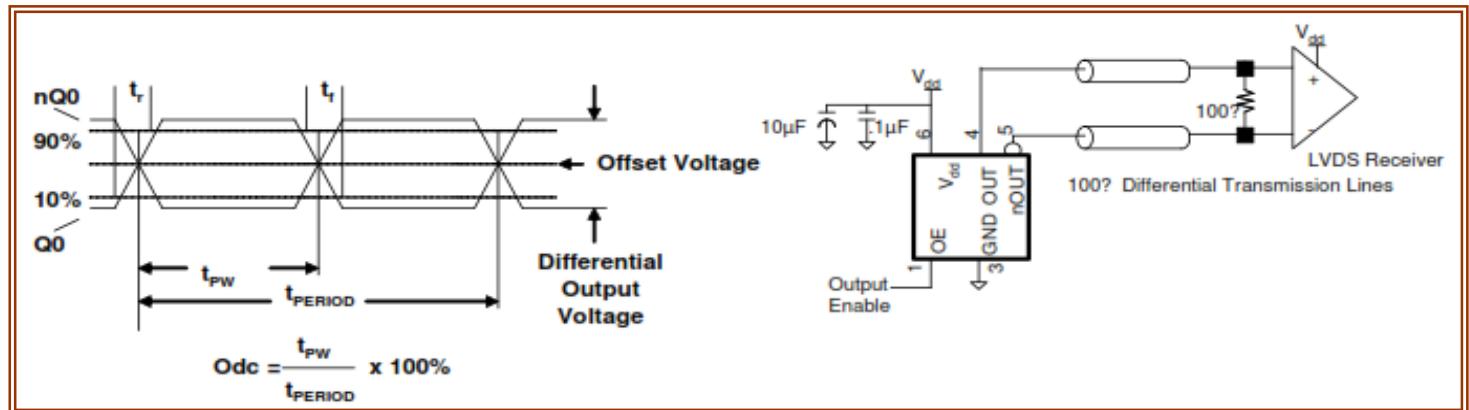


Figure 11. 3.3V or 2.5V LVDS waveform measurement test setup

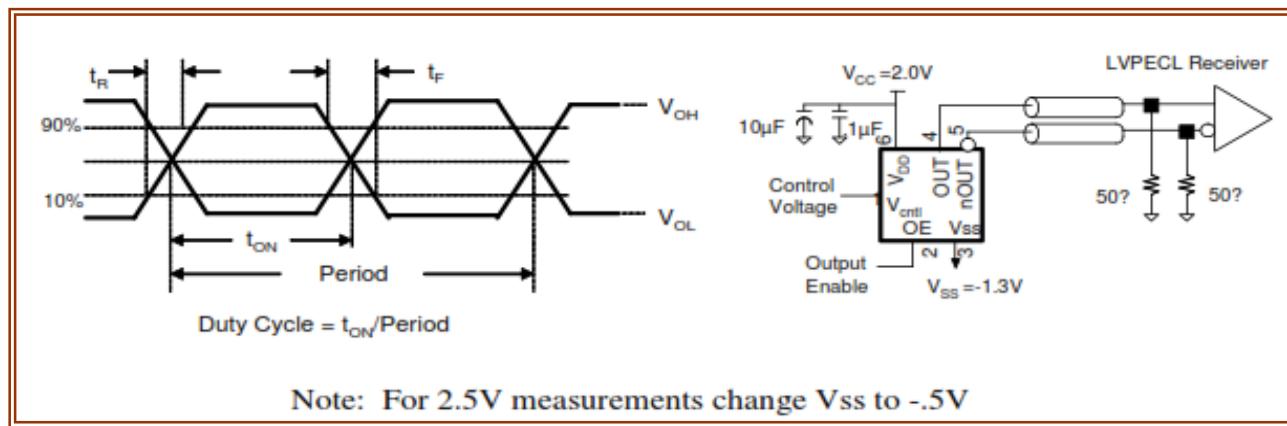


Figure 12. 3.3V LVPECL waveform measurement test setup

Application Information

Termination for 3.3V LVPECL Output

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts offered are recommended only as guidelines.

OUT and nOUT are low impedance following outputs that generate LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figures 13 and 14 present two different designs. They are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designer simulate to guarantee compatibility across all printed circuit and clock component process variations.

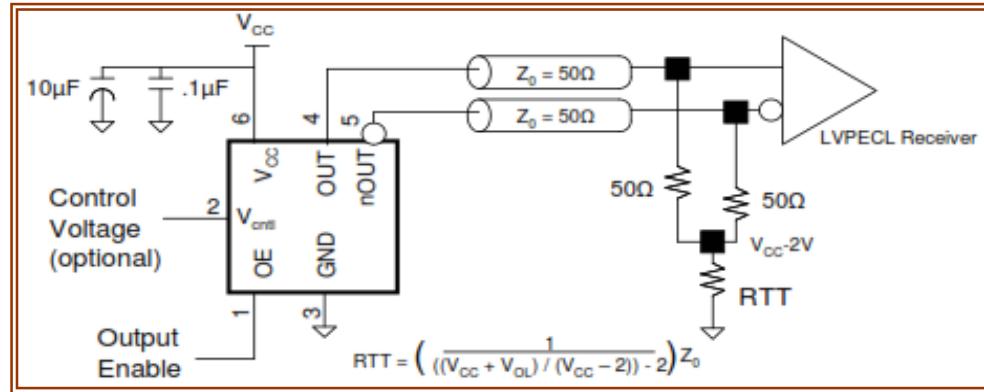


Figure 13. 3.3V LVPECL XO Application Schematic & Power Supply Decoupling

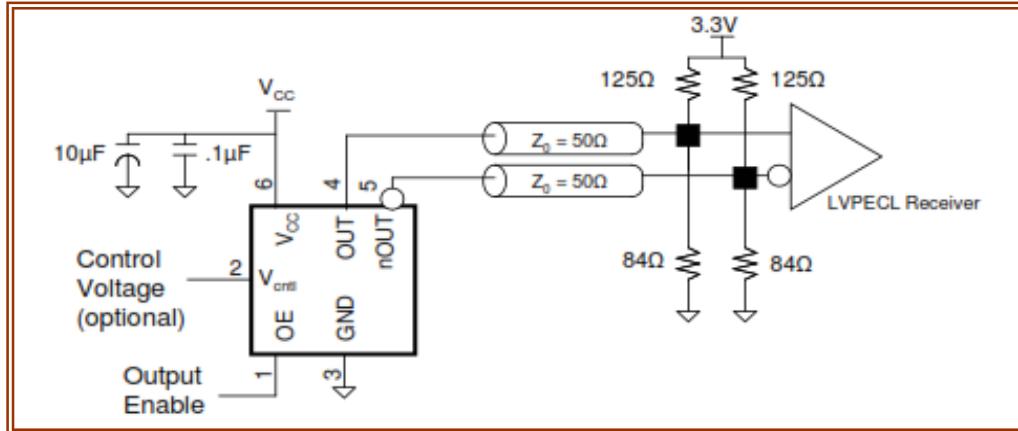


Figure 14. Alternante 3.3V LVPECL XO Application Schematic & Power Supply Decoupling

Termination for 2.5V LVPECL Output

Figure 15-17 shows examples of termination for 2.5V LVPECL drivers. These terminations are equivalent to terminating 50Ω to VCC-2V. For VCC = 2.5V, the VCC-2V is very close to ground level. The 18Ω in Figure 16 can be eliminated and termination is shown in Figure 17.

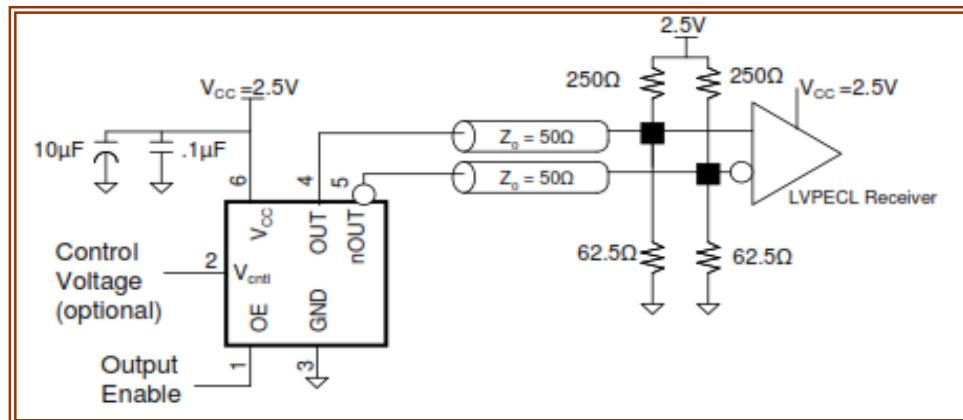


Figure 15. 2.5V LVPECL XO Drive Termination Example

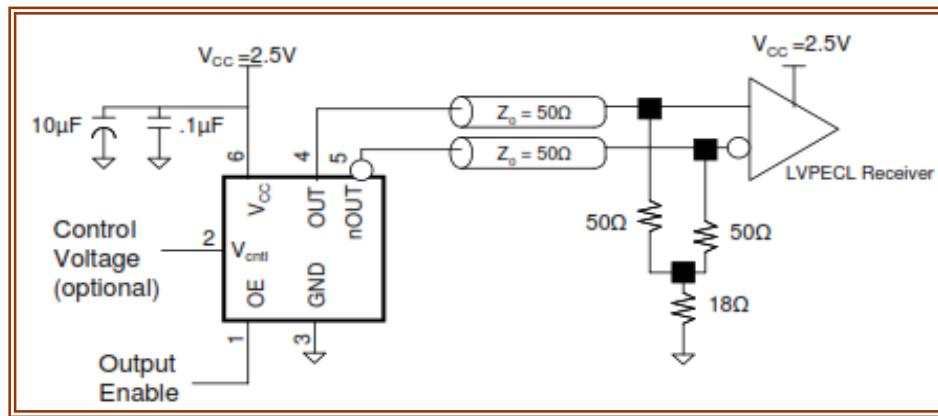


Figure 16. Alternate 2.5V LVPECL XO Drive Termination Example

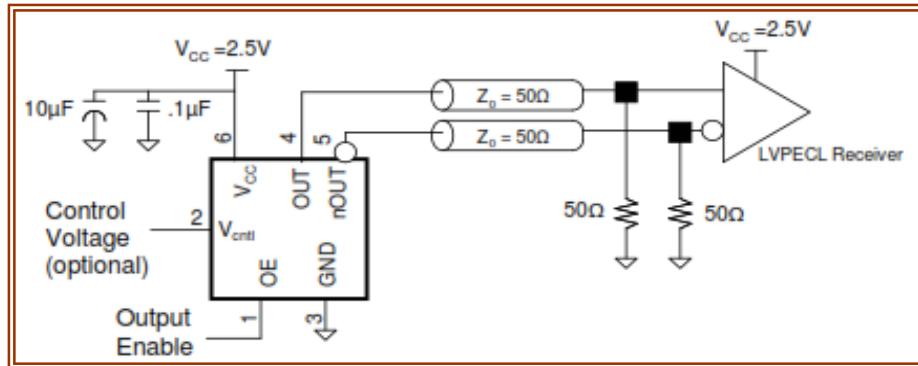


Figure 17. Alternate 2.5V LVPECL XO Drive Termination Example

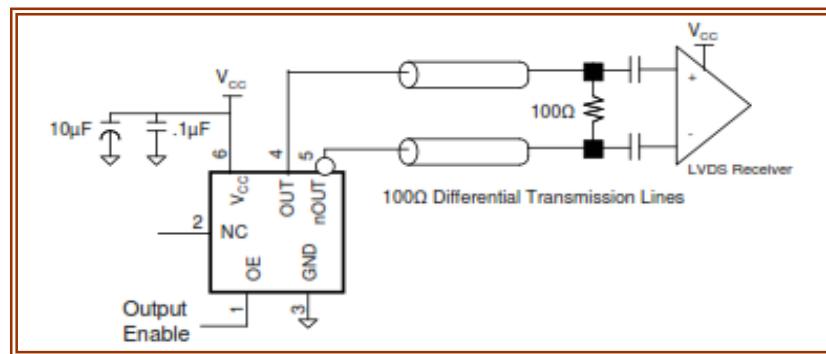


Figure 18. Termination for 3.3V and 2.5V LVDS Output

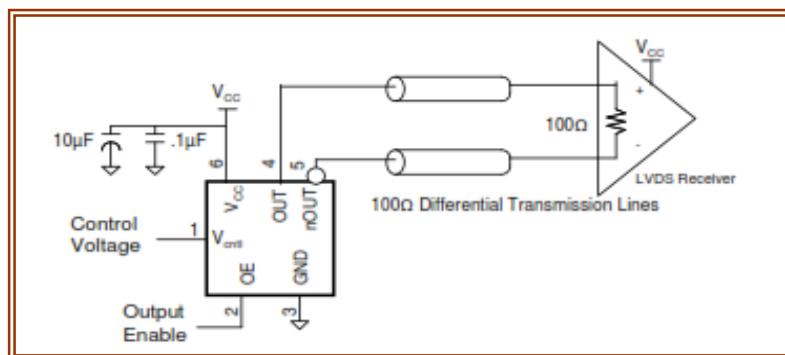
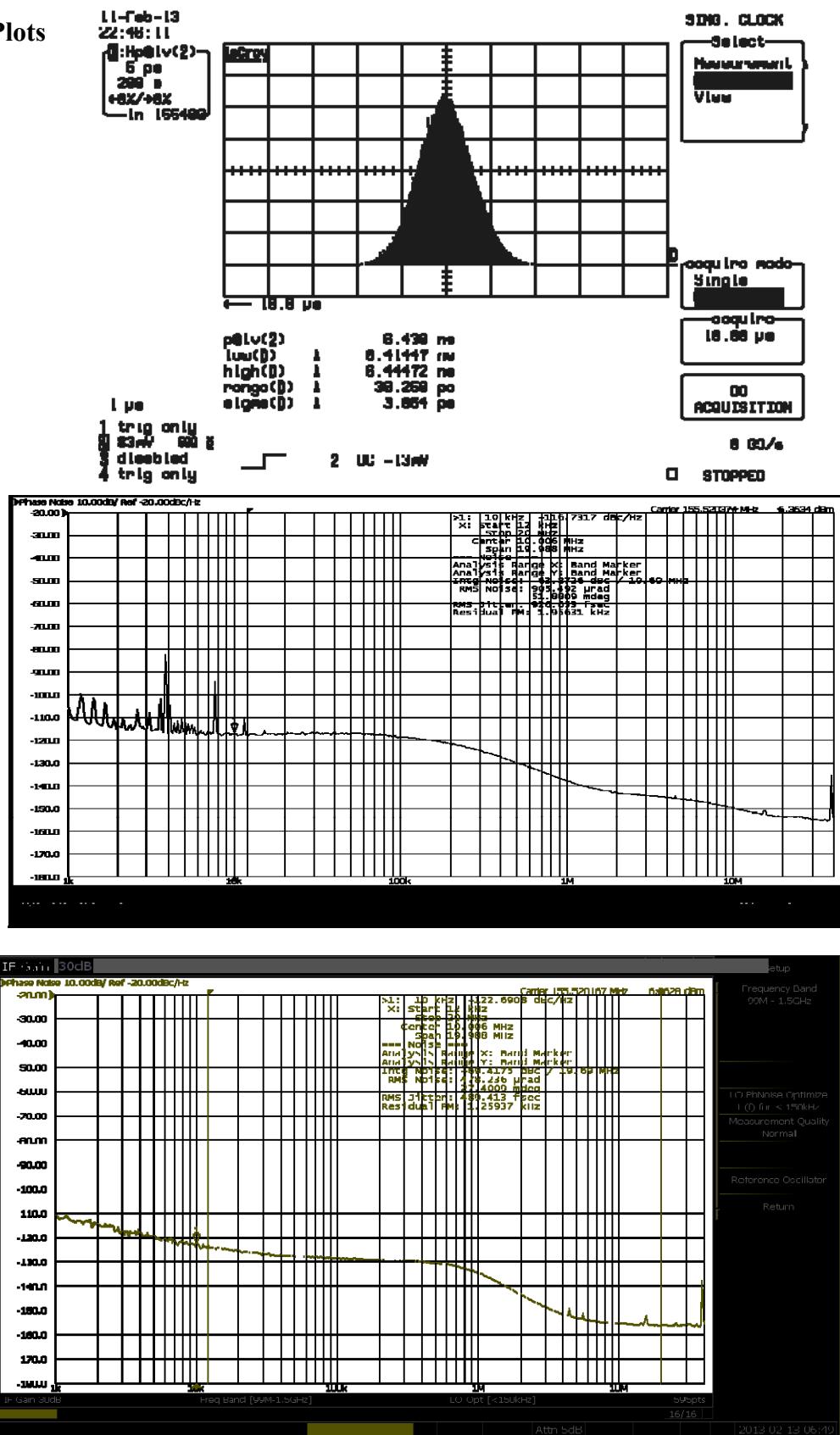


Figure 19. 3.3V and 2.5V LVDS XO Application Schematic & Power Supply Decoupling

CARDINAL COMPONENTS, INC.

CJVYE/ CJVYL 750MHz - 1500MHz

Phase Noise & Jitter Plots



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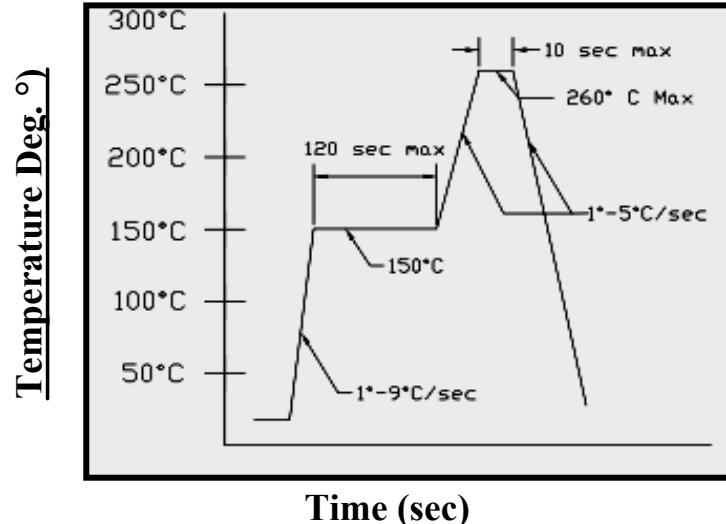
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Tel: (973)785-1333
E-Mail: sales@cardinalxtal.com
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CJVYE/ CJVYL 750MHz - 1500MHz

Recommended Solder Profile for
Cardinal Components, Inc.
Package Infared Reflow.
Do Not Use Ultrasonic-Wave Soldering or
Wave Solder with Package Immersed in Solder
Damage to Crystal will result.



Reliability

Cardinal Components Inc., qualification includes aging at various extreme temperatures, shocks and vibration, temperature cycling, and IR reflow simulation. The Cappuccino family meets the following qualification tests:

Environmental Compliance	
Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2016
Moisture Sensitivity Level	IPC/ JEDEC J-STD-020, MSL1

Handling Precautions

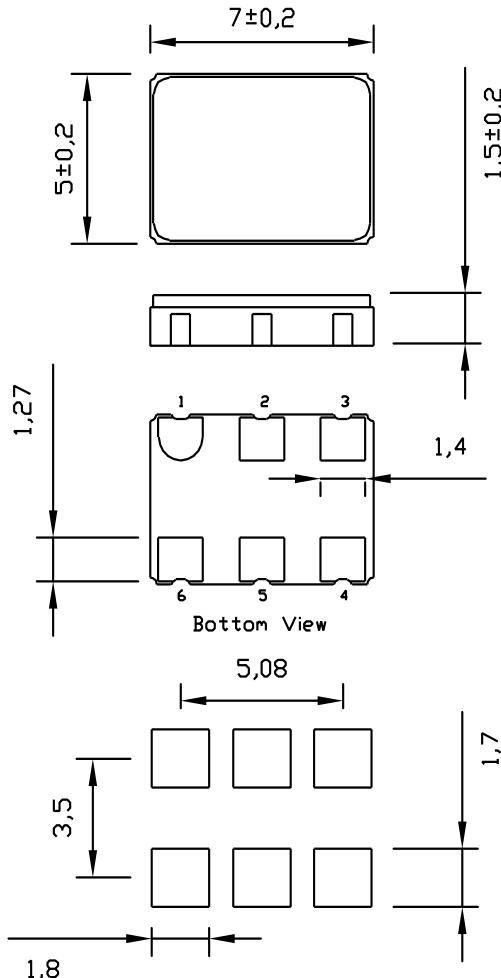
Although ESD protection circuitry has been designed into the Cappuccino proper precautions should be taken when handling and mounting. Cardinal employs a human body model (HBM) and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation.

ESD Ratings		
Model	Minimum	Conditions
Human Body Model	1000V	MIL-STD-883, Method 3015
Charged Device Model	900V	JEDEC, JESD22-C101
Machine Model	200V	JEDEC, JESD22-A115-A

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CJVYE/ CJVYL 750MHz - 1500MHz

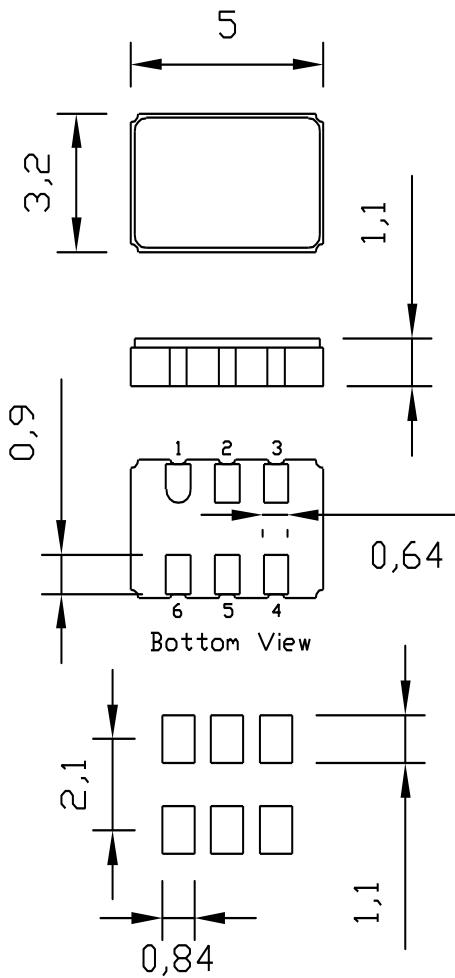
Style 7: 5x7mm



6 Pad LVDS/LVPECL

Pin 1	VC
Pin 2	OE
Pin 3	GND
Pin 4	OUT
Pin 5	nOUT
Pin 6	V _{DD}

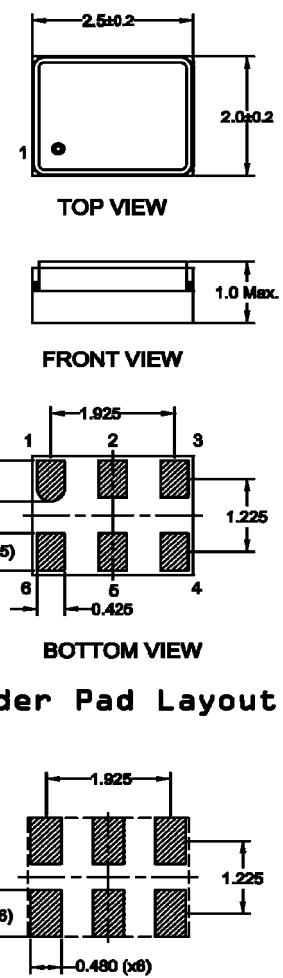
Style 5: 5x3.2mm



6 Pad LVDS/LVPECL

Pin 1	VC
Pin 2	OE
Pin 3	GND
Pin 4	OUT
Pin 5	nOUT
Pin 6	V _{DD}

Style 2: 2.5 X 2 mm



Solder Pad Layout

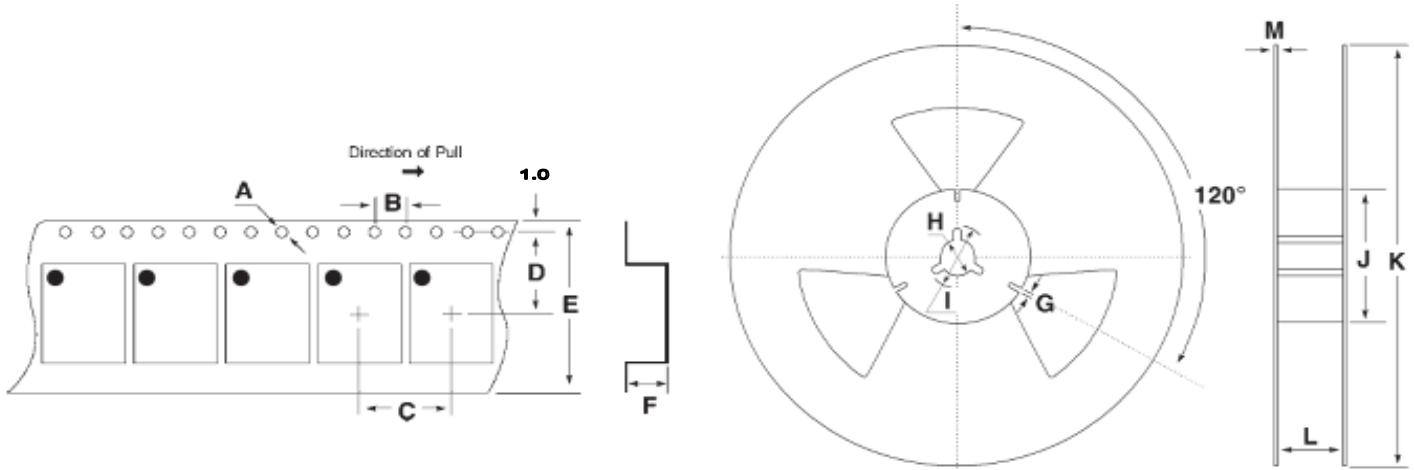
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Wayne, NJ 07470

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Tape and Reel Specifications



Tape Specifications (mm)

Package	A	B	C	D	E	F	QTY
2 = 2.5 X 2	1.5	4.0	4.0	3.5	8.0	1.1	1,000
5 = 5 X 3.2	1.5	4.0	8.0	5.5	12.0	1.8	1,000
7 = 7 X 5	1.5	4.0	8.0	7.5	16.0	2.2	1,000

Reel Specifications (mm)

Package	G	H	I	J	K	L	M
2 = 2.5 X 2	2.0	13	21	60	180	9.0	1.8
5 = 5 X 3.2	2.0	13	21	60	180	13.0	1.25
7 = 7 X 5	2.0	13	21	60	180	17.0	1.25