

Differential LVPECL Clock Oscillator

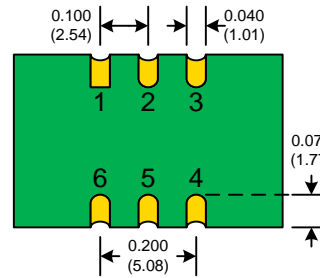
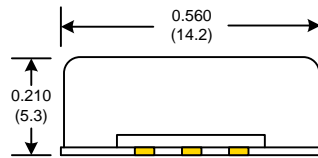
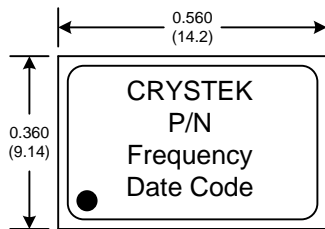


CCPD-920 Model 9x14 mm SMD, 3.3V, LVPECL

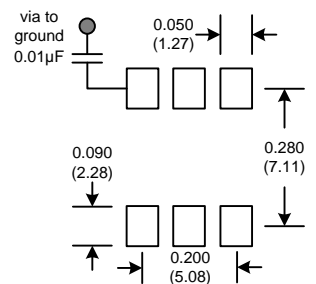
Frequency Range:	50 MHz to 150 MHz
Frequency Stability:	±20, ±25, ±50ppm (0°C to 70°C) ±25, ±50ppm (-40°C to 85°C)
Temperature Range:	0°C to 70°C -40°C to 85°C (Option X)
Storage:	-45°C to 90°C
Input Voltage:	3.3V ± 0.3V
Input Current:	88mA Max
Output:	Differential LVPECL
Symmetry:	45/55% Max @ zero crossing point
Rise/Fall Time:	1ns Max (20% to 80%)
Linearity:	± 10% Max
Logic:	Terminated to Vdd-2V into 50 ohms Logic "0" "0" = Vcc-1.85V Min, Vcc-1.62V Max Logic "1" "1" = Vcc-1.02V Min, Vcc-0.81V Max
Disable Time	200ns Max
Start-up Time	1ms Typical, 2ms Max
Phase Jitter:	12kHz to 80MHz 0.5psec Typical, 1psec RMS Max
Phase Noise:	10Hz -65 dBc/Hz Typical 100Hz -98 dBc/Hz Typical 1kHz -125 dBc/Hz Typical 10kHz -140 dBc/Hz Typical 100kHz - 100MHz -145 dBc/Hz Typical
Aging:	<3ppm 1 st year, <1ppm every year thereafter



Designed to meet today's requirements for 3.3V Differential LVPECL applications. The CCPD-920 is produced using our cost saving FR5 PCB and UM-1 overtone crystal technology. This design offers considerable cost savings over other HFF XO's products. Also available in 14 pin dip fully hermetic package.



SUGGESTED PAD LAYOUT



RECOMMENDED REFLOW SOLDERING PROFILE

900034 (See App Note listed on website)

<http://www.crystek.com/specification/reflow/900034.pdf>

Crystek Part Number Guide

CCPD-920 X - 25 - 100.000

#1 #2 #3 #4 #5

#1 Crystek 9x14 SMD PECL OSC
#2 Model 920
#3 Temp. Range: Blank = 0/70°C, X=-40/85°C
#4 Stability: (see Table 1)
#5 Frequency in MHz: 3 or 6 decimal places

Stability Indicator

20 = 0/70°C (±20ppm)
25 = 0/70°C (±25ppm)
50 = 0/70°C (±50ppm)
25 = -40/85°C (±25ppm)
50 = -40/85°C (±50ppm)

Example:
CCPD-920X-25-100.000 = 3.3V, 45/55, -40/85°C, 25ppm, 100.000 MHz

Table 1

PIN	Function	Tri-State Function	
		Function pin 2	Output pin
1	NC	Open	Active
2	E/D	"0" level Vcc-1.620V Max	Active
3	GND	"1" level Vcc-1.025V Min	High Z
4	OUT	Disabled State:	
5	COU	Pin 4 will assume a fixed level of logic "0"	
6	Vdd	Pin 5 will assume a fixed level of logic "1"	

Specifications subject to change without notice.

TD-051101 Rev. G