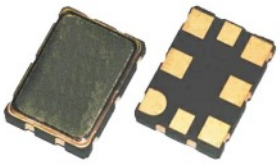
FEATURES

- **EQJF Series oscillators, Ultra-low Jitter**
- **Outputs LVPECL, LVDS, CML Differential outputs: 50~2100MHz**
- **HCSL Differential Outputs: 50~700MHz**
- **RMS phase jitter 150fs ftypical**
- **ITAR Free**



ITAR FREE

GENERAL SPECIFICTIONS

Output Logic Type	LVPECL	LVDS	CML	HCSL
Frequency Range	50 ~ 2100MHz	50 ~ 2100MHz	50 ~ 2100MHz	50 ~ 700MHz
Load	50Ω into VDD-2V or Thevenin equivalent	100Ω between OUT and OUTN	50Ω to VDD	50Ω to GND
Power Supply Voltage (VDD)	+2.5V±10% or +3.3V±10%	+2.5V±10% +3.3V±10%	+1.8V±5% +2.5V±10% +3.3V±10%	+1.8V±5% or +2.5V±10% or +3.3V±10%
Output 'HIGH' Voltage	VDD-1.165V min. VDD-0.8V max.	VDD: 1.4V typical VDD: 1.6V max.	VDD: -0.085V min. VDD: = max.	VDD: 0.66V min. VDD: 1.15V max.
Output 'LOW' Voltage	VDD: -2.0V min. VDD: -1.55V max.	VDD: 1.1V typical VDD: 0.9V min.	VDD: -0.6V min. VDD: -0.32V min.	VDD: 0.0V min. VDD: 0.15V min.
Frequency Stability Codes	Frequency stability over operating temp. Range	±25ppm	±50ppm	±100ppm
	Commercial -10° to +70°C	A	B	C
	Industrial -40° to 85°C	D	E	F

If non-standard please enter the desired stability after the 'C' or 'I'
Example:
'C20' is ±20ppm over -10° to +70°C.

Ageing at Ta = 25°C	±3ppm max. first year; 2±ppm max. per year thereafter			
Duty Cycle	50%±5%	50%±5%	50%±5%	50%±5%
Rise Time (Tr) **Fall Time (Tf)** (20% ~ 80% waveform)	0.35ns max.	0.35ns max.	0.35ns max.	0.4ns max.
Current Consumption at VDD = 3.3V	100mA typical 120mA max.	75mA typical 90mA max.	70mA typical 85mA max.	94mA typical 115mA max.
Current with output Disabled	99mA max.	74mA max.	69mA max.	93mA max.

SPECIFICATION

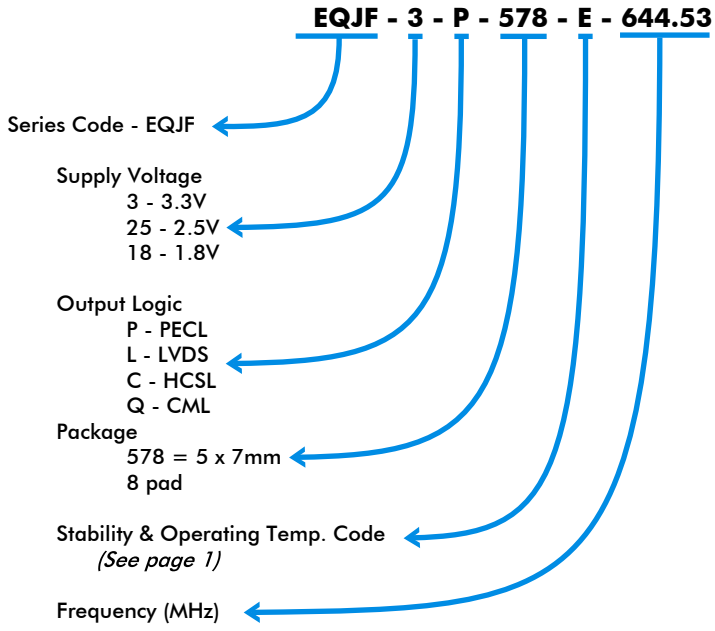
Phase Jitter, rms: (12kHz to 20MHz)	150fs typical, 300fs max.
Start-up Time:	5ms typical; 10ms max.
OE Control	
To Enable:	0.8% of VDD min. or no connection
To Disable:	0.2% of VDD max. (high impedance)
Output Enable Time:	2.5ms max.
Output Disable Time:	10μs max.

ENVIRONMENTAL PERFORMANCE SPECIFICATION

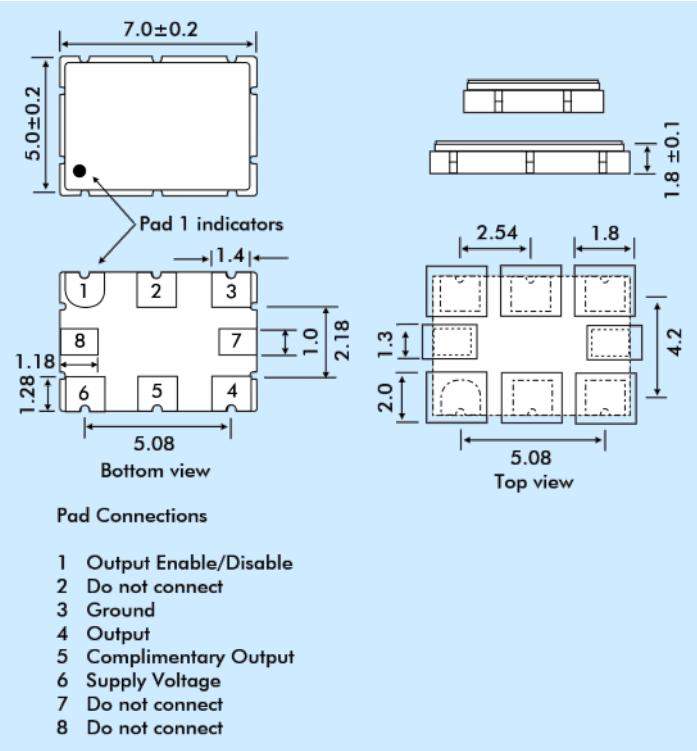
Green Requirement	ROHS Compliant, pB (lead) free in accordance with EU Directive 2002/95/EC 6/6 (2002/95/EC) and WEEE (2002/96/EC)
Second Level Interconnect	e4
Moisture Sensetivity Level	Level 1 (infinite) according to IPC/JEDEC J-STD-020D.1
Storage Temperature Range	-55° to +150°C
Humidity	85% RH, 85°C, 48 hours
Fine Leak	MIL-STD-883 Method 1014, condition A
Gross Leak	MIL-STD-883 Method 1014, condition C
Solderability	MIL-STD-202F Method 208E
Reflow	260°C for 10 seconds, twice
Vibration	MIL-STD-202F Method 204, 35G, 50 to 2000Hz
Shock	MIL-STD-202F Method 213B, test cond. E, 1000g ½ sine wave
Resistance to Solvent	MIL-STD-202F Method 215
Temperature Cycling	MIL-STD-883 Method 1010
ESD Rating	Human body model (HBM): 2000V min.
Pad Surface Finish	Gold (0.3µm to 1.0µm) over nickel (1.27µm to 8.89µm)
Weight of Device	0.045 gm typical

PART NUMBERING

EQJF oscillator part numbers are configured as per the following example: EQJF-3-P-578-E-644.53



OUTLINE & DIMENSIONS



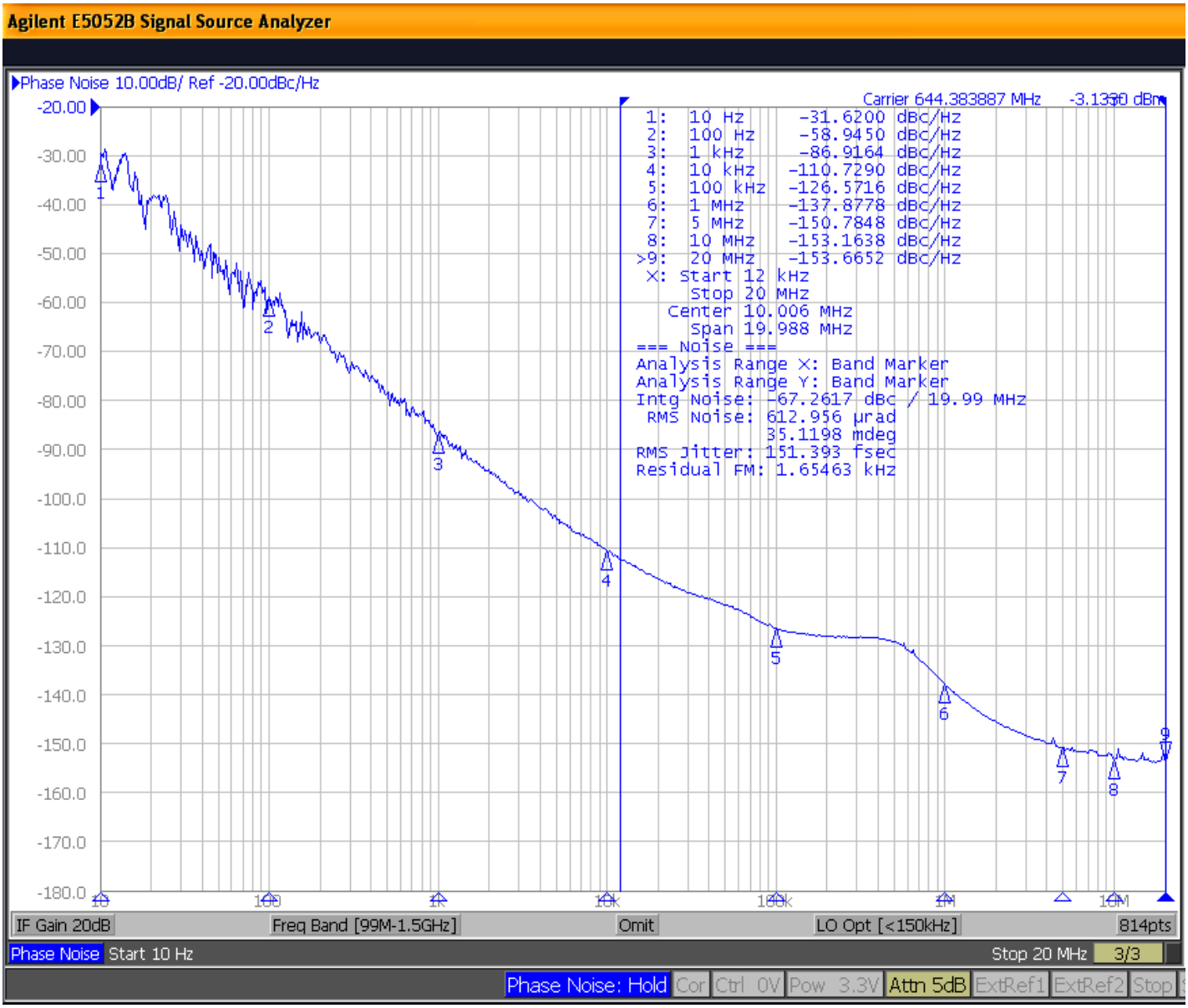
Pad Connections

1 Output Enable/Disable
2 Do not connect
3 Ground
4 Output
5 Complimentary Output
6 Supply Voltage
7 Do not connect
8 Do not connect

EQJF578 PHASE NOISE & PHASE JITTER (Typical) VDD = +3.3V, Output Enable +3.3V

SSB Phase Noise Data (dBc/Hz Typical)	**Frequency (MHz)**	156.25	491.52	644.53	1480	2100
	10Hz offset	-39	-16	-31	-12	-18
	100Hz offset	-74	-48	-58	-54	-49
	1kHz offset	-99	-83	-86	-80	-77
	10kHz offset	-123	-112	-110	-104	-100
	100kHz offset	-139	-128	-126	-119	-116
	1MHz offset	-149	-140	-137	-130	-125
	5MHz offset	-156	-151	-150	-145	-141
	10MHz offset	-157	-153	-153	-148	-145
	20MHz offset	-157	-154	-153	-150	-147
Phase Jitter fs (12kHz~20MHz RMS)		159	155	151	147	163

PHASE NOISE PLOT OF EQJF-3-P-578-E-150N-644.53 (Typical) VDD = +3.3V, Output Enable = +3.3V



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