PECL/LVDS

Features

- Typical 7.0 x 5.0 x 1.7 mm 6 pads ceramic SMD package.
- Tight symmetry (45 to 55%) available.
- Wide frequency control range.
- Low phase jitter (Max: 1.0pS).
- Complementary Output.
- Non-Multi Type

Specifications

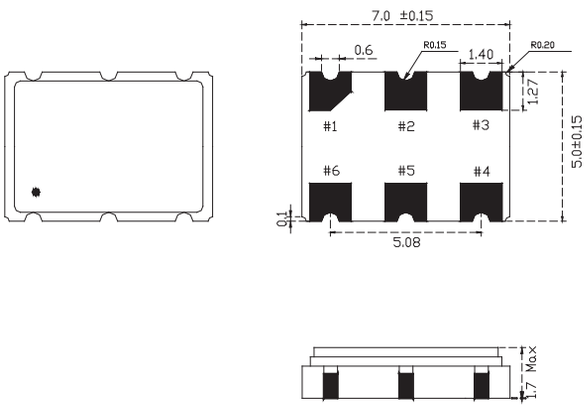
Output Logic	PECL				LVDS				Unit
Parameter	Min.		Max.		Min.		Max.		
	3.3	2.5	3.3	2.5	3.3	2.5	3.3	2.5	V
Supply Voltage Variation(VDD) 5%	3.135	2.375	3.465	2.625	3.135	2.375	3.465	2.625	
Frequency Range	25.0		250		12.5		250		MHz
Standard Frequency	155.520								MHz
Operating Temp. Range	-40 ~ +85								℃
Frequency Stability*	25								ppm
Supply Current									
PECL 25.0MHz ≤ Fo < 250MHz	-		100		-				mA
LVDS 12.5MHz ≤ Fo < 250MHz							80		
Output Level									
Output High (Logic "1")	2.28	1.48	-		1.375				V
Output Low (Logic "0")	-		1.67	0.87			1.125		
Transition Time- Rise/Fall Time+	-		1.0		-		1.0		nS
Start up Time	-		10		-		10		mSec
Output Load	50 Ohms to Vcc-2.0V				100Ω Between the two outputs				Ohms
Tri-State(Input to Pin 1)									
Output Active	0.7*Vcc				0.7*Vcc				V
Output in High Impedance State			0.3*Vcc				0.3*Vcc		
Phase Jitter(12Khz ~ 20Mhz)	-		1.0		-		1.0		pS
Storage Temp. Range	-55		125		-55		125		℃

Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.

*inclusive of calibration @ 25℃, operating temperature range, input voltage variation, load variation, aging, shock, and vibration.

+Transition times are measured between 10% and 90% of VDD, with an output load of 15pF.

DIMENSION (Unit: mm)



Pin Connection

1:	E/D
2:	N/C
3:	GND
4:	Output Q
5:	Output Q'
6:	+VDD