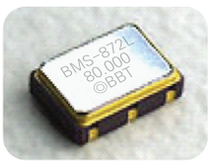
PECL/LVDS

Features



- •Advanced PLL Multiplication Techniques
- •+3.3Vdc Operation
- •Frequency Range 12.0 ~ 400MHz.
- •Output Enable Standard.
- •Standard 7mm x 5mm 6-Pad Surface Mount Footprint.
- •Tape & Reel Packaging

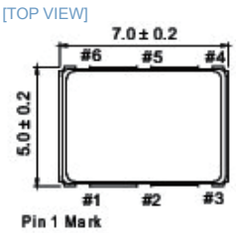
Specifications

Output Logic	PECL		LVDS		Unit
Parameter	Min.	Max.	Min.	Max.	
	3.3V		3.3V		V
Supply Voltage Variation(VDD) 5%	3.135	3.465	3.135	3.465	
Frequency Range	12.0	400	12.0	400	MHz
Standard Frequency	155.520				MHz
Operating Temp. Range	-40 ~ +85				℃
Frequency Stability*	25				ppm
Supply Current					
PECL 12.0MHz ≤ Fo < 400MHz	-	100	-		mA
LVDS 12.0MHz ≤ Fo < 400MHz				80	
Output Level					
Output High (Logic "1")	2.28	-	1.375		V
Output Low (Logic "0")	-	1.67		1.125	
Transition Time- Rise/Fall Time+	-	1.0	-	1.0	nS
Start up Time	-	10	-	10	mSec
Output Load	50 Ohms to Vcc-2.0V		100Ω Between the two outputs		Ohms
Tri-State(Input to Pin 1)					
Output Active	0.7 VDD		0.7 VDD		V
Output in High Impedance State		0.3 VDD		0.3 VDD	
Phase Jitter(12Khz ~ 20Mhz)	-	3.0	-	3.0	pS
Storage Temp. Range	-55	125	-55	125	℃

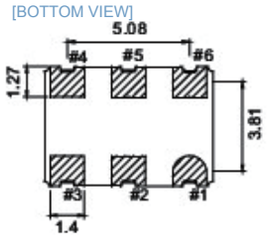
Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.

DIMENSION (Unit: mm)

[TOP VIEW]

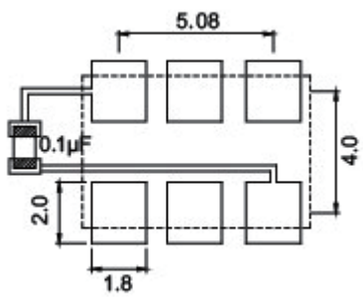


[BOTTOM VIEW]



[SIDE VIEW]

SOLDER PAD LAYOUT(mm)



Pin Connection

1:	E/D
2:	N/C
3:	GND
4:	Output Q
5:	Output Q'
6:	+VDD