

LVDS 7 x 5 x 1.8mm SMD

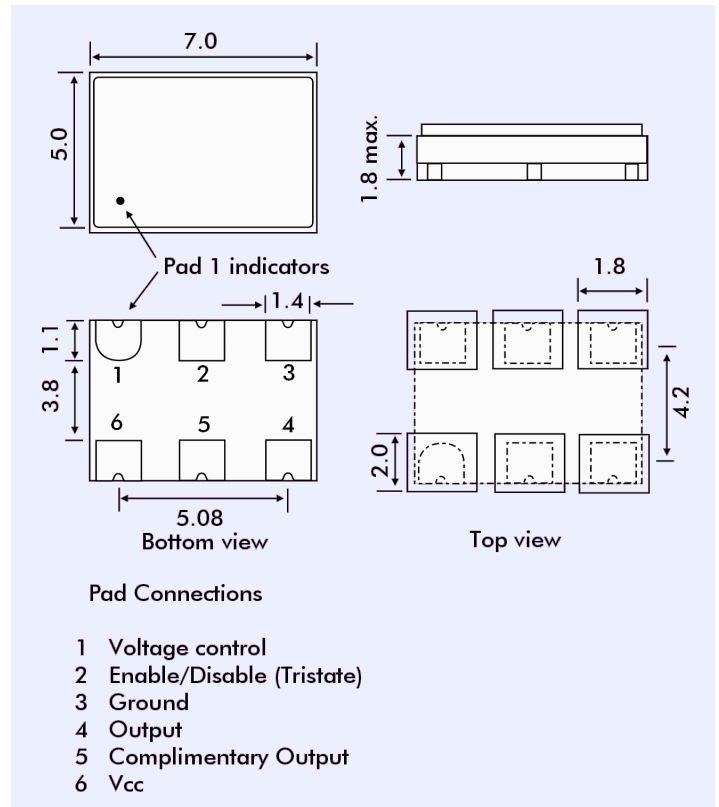
- Frequency range 38MHz to 640MHz
- LVDS Output
- Supply Voltage 3.3 VDC
- Integrated Phase Jitter less than 1ps typical



GENERAL SPECIFICATION

Model:	'GDF' Series
Technology:	High Q fundamental crystal with low jitter multiplier circuit
Output Logic:	LVDS
Frequency range:	38.0MHz to 640.0MHz
Supply Voltage (V _{dd}):	+3.3V ±5% (Part code = '3')
Output Logic High '1':	1.4V typical, 1.6V max.
Output Logic Low '0':	0.9V minimum, 1.1V typical
Differential Output Voltage:	247mV min., 355mV typ., 454mV max. Output1 - Output 2
Differential Output Error:	-50mV min., 50mV max.
Output Offset Voltage:	1.125V min., 1.200V typ. 1.375V max.
Offset Magnitude Error:	0mV min., 3mV typ., 25mV max.
Integrated Phase Jitter:	0.4ps typical, 0.5ps max. (for 156.250MHz)
Period Jitter RMS:	3ps typical, 5ps max.
Period Jitter Peak to Peak:	20ps typical, 30ps max.
Frequency Stability:	See table
Current Consumption	
38MHz to 100MHz:	45mA max.
100MHz to 320MHz:	60mA max.
320MHz to 640MHz:	70mA max.
Rise/Fall Times:	0.7ns typ., 1 ns max. (from 20% to 80% waveform)
Load:	50Ω from each output
Start-up Time:	5ms typical, 10ms max.
Duty Cycle:	50%±5% measured at V _{DD} -1.3V
Ageing:	±3ppm max. first year, ±2ppm/year thereafter
Control Voltage Centre:	+1.65V, V _{CON} = 0.3V to 3.0V
Frequency Deviation Range:	±80ppm (min.)
Linearity:	6% typical, 10% max.
Slope Polarity:	Positive. Increase of control voltage increases output frequency
Modulation Bandwidth:	25kHz min.
Input Impedance:	60kΩ min.
Enable/Disable:	See below

OUTLINE AND DIMENSIONS



FREQUENCY STABILITY OVER TEMPERATURE

Frequency Stability over Operating Temp. Range*	±25ppm	±50ppm	±100ppm
Commercial -10° to +70°C	A	B	C
Industrial -40 to +85°C	D	E	F

* If non-standard temperature stability is required enter the desired stability in ppm after either 'C' (-10° to +70°) or 'I' (-40° to +85°C)
 Example: 'C20' = ±20ppm over -10 to +70°C

PHASE NOISE at 156.250MHz

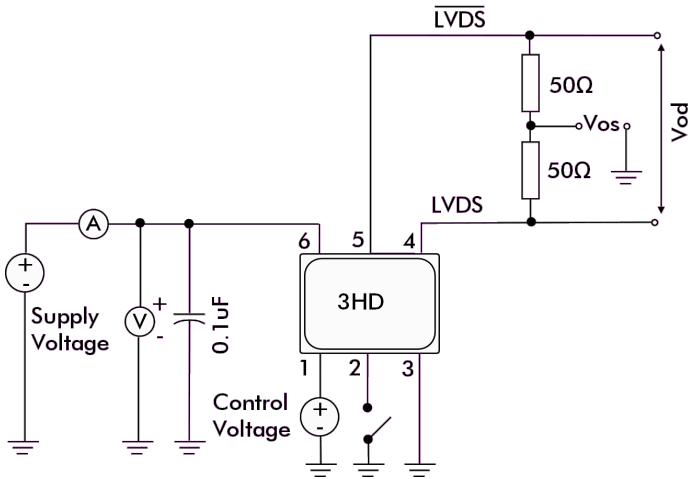
Offset	Value
10Hz	-62 dBc/Hz
100Hz	-92 dBc/Hz
1kHz	-120 dBc/Hz
10kHz	-132 dBc/Hz
100kHz	-128 dBc/Hz
1MHz	-140 dBc/Hz
10MHz	-150 dBc/Hz

ENABLE/DISABLE FUNCTION (PAD2)

No Connection:	Differential LVDS and complimentary LVDS outputs enabled.
Disable:	Both outputs are disable (high impedance) when Pad 2 is taken below 0.45V ref to ground. Oscillator is always on, only output buffer stage is disabled.
Enable:	Both outputs are enabled when Pad 2 is take above 1.45V ref to ground.
Enable/Disable Time:	10ns max.

LVDS 7 x 5 x 1.8mm SMD

LVDS VCXO TEST CIRCUIT



PART NUMBER SCHEDULE

Example: 3GDF576B-100N-156.250

Supply Voltage +3.3V

Series Designator GDF576

Stability over Temperature Range

A = ± 25 ppm over -10° to $+60^{\circ}$ C

B = ± 50 ppm over -10° to $+60^{\circ}$ C

C = ± 100 ppm over -10° to $+60^{\circ}$ C

D = ± 25 ppm over -40° to $+85^{\circ}$ C

E = ± 50 ppm over -40° to $+85^{\circ}$ C

F = ± 100 ppm over -40° to $+85^{\circ}$ C

Pullability in \pm ppm

Pullability Determinator

N = minimum

M = maximum

T = Typical

Frequency in MHz