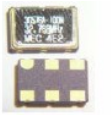
LVDS 7 x 5 x 1.8mm SMD

- **Frequency range 750kHz to 800.0MHz**
- **LVDS Output**
- **Supply Voltage 3.3 VDC**
- **Integrated Phase Jitter less than 2.6s typical**
- **Low cost unit**

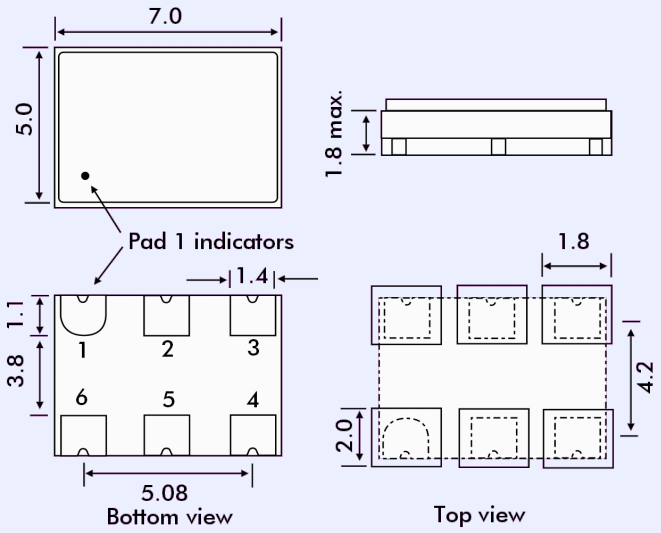
RoHS



GENERAL SPECIFICATION

Model:	'GDW' Series
Technology:	High Q fundamental crystal with multiplier circuit
Output Logic:	LVDS
Frequency range:	750.0kHz to 800.0MHz
Supply Voltage (Vdd):	+3.3V ±5% (Part code = '3')
Output Logic High '1':	1.4V typical, 1.6V max.
Output Logic Low '0':	0.9V minimum, 1.1V typical
Differential Output Voltage:	247mV min., 355mV typ., 454mV max. Output1 - Output 2
Differential Output Error:	-50mV min., 50mV max.
Output Offset Voltage:	1.125V min., 1.200V typ. 1.375V max.
Offset Magnitude Error:	0mV min., 3mV typ., 25mV max.
Integrated Phase Jitter:	2.6ps typical, 4ps max. (for 155.520MHz)
Period Jitter RMS:	4.3ps typical
Period Jitter Peak to Peak:	27ps typical
Phase Noise:	*See table*
Frequency Stability:	*See table*
Current Consumption	
<24MHz:	25mA max.
24.01MHz to 96MHz:	45mA max.
96.01MHz to 800MHz:	80mA max.
Rise/Fall Times:	1.5ns max. (from 20% to 80% waveform)
Load:	50Ω from each output
Start-up Time:	5ms typical, 10ms max.
Duty Cycle:	50%±5% measured at V_{DD} -1.3V
Ageing:	±3ppm max. first year, ±2ppm/year thereafter
Control Voltage Centre:	+1.65V, V_{CON} = 0.3V to 3.0V
Frequency Deviation Range:	±80ppm (min.)
Linearity:	6% typical, 10% max.
Slope Polarity:	Positive. Increase of control voltage increases output frequency
Modulation Bandwidth:	25kHz min.
Input Impedance:	2MΩ min.
Enable/Disable:	*See below*

OUTLINE AND DIMENSIONS



Pad Connections

1 Voltage control
2 Enable/Disable (Tristate)
3 Ground
4 Output
5 Complimentary Output
6 Vcc

FREQUENCY STABILITY OVER TEMPERATURE

Frequency Stability over Operating Temp. Range*	±25ppm	±50ppm	±100ppm
Commercial -10° to +70°C	A	B	C
Industrial -40 to +85°C	D	E	F

** If non-standard temperature stability is required enter the desired stability in ppm after either 'C' (-10° to +70°) or 'I' (-40° to +85°C) Example: 'C20' = ±20ppm over -10 to +70°C*

PHASE NOISE at 155.520MHz

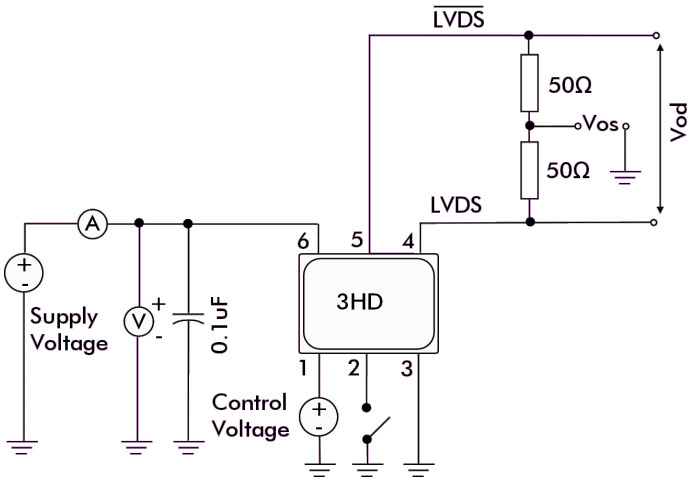
Offset	Value
10Hz	-60 dBc/Hz
100Hz	-90 dBc/Hz
1kHz	-115 dBc/Hz
10kHz	-125 dBc/Hz
100kHz	-119 dBc/Hz
1MHz	-120 dBc/Hz
10MHz	-140 dBc/Hz

ENABLE/DISABLE FUNCTION (PAD2)

No Connection:	Differential LVDS and complimentary LVDS outputs enabled.
Disable:	Both outputs are disable (high impedance) when Pad 2 is taken below 0.45V ref to ground. Oscillator is always on, only output buffer stage is disabled.
Enable:	Both outputs are enabled when Pad 2 is take above 1.45V ref to gound.
Enable/Disable Time:	10ns max.

LVDS 7 x 5 x 1.8mm SMD

LVDS VCXO TEST CIRCUIT



PART NUMBER SCHEDULE

Example: 3GDW576B-100N-155.520

Supply Voltage +3.3V

Series Designator GDW576

Stability over Temperature Range
- A = ±25ppm over -10° to +60°C
- B = ±50ppm over -10° to +60°C
- C = ±100ppm over -10° to +60°C
- D = ±25ppm over -40° to +85°C
- E = ±50ppm over -40° to +85°C
- F = ±100ppm over -40° to +85°C

Pullability in ±ppm

Pullability Determinator
- N = minimum
- M = maximum
- T = Typical

Frequency in MHz