

## High Frequency 8 pin Dual-in-Line

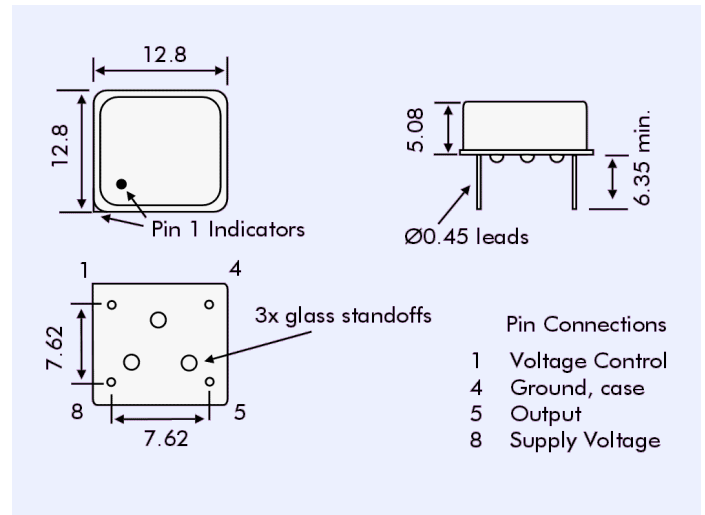
- Frequency range 50.0MHz to 320.0MHz
- CMOS/TTL Output
- Supply Voltage 3.3 VDC
- Integrated Phase Jitter less than 1ps



### GENERAL SPECIFICATION

Model:	'GF' Series
Technology:	High Q fundamental crystal with ultra-low jitter multiplier circuit
Output Logic:	LVCMS0
Frequency range	
With 15pF load:	50.01MHz to 200.0MHz
With 10pF load:	50.01MHz to 320.0MHz
Supply Voltage (Vdd):	+3.3V $\pm$ 5% (Part code = '3')
Output Logic High '1':	90% Vdd min.
Output Logic Low '0':	10% Vdd max.
Integrated Phase Jitter:	0.4ps typical, 0.5ps max. (for 156.25MHz)
Period Jitter RMS:	3ps typical 5ps max.
Period Jitter Peak to Peak:	20ps typical 30ps max. (with decoupling capacitor between Vdd and ground)
Phase Noise:	See table
Current Consumption	
< 100MHz:	30mA max.
> 100MHz:	40mA max.
Rise/Fall Times:	0.7ns typical 0.3V~3.0V, 15pF load
Frequency Stability:	See table
Frequency Deviation Range:	$\pm$ 80ppm (standard)
Load:	15pF
Start-up Time:	10ms max., 5ms typical
Duty Cycle:	50% $\pm$ 5% measured at 50% Vdd
Linearity:	6% typical, 10% max.
Modulation Bandwidth:	25kHz min.
Input Impedance:	60k $\Omega$ min.
Slope Polarity:	Monotonic and positive (An increase of control voltage increases output frequency.)
Ageing:	$\pm$ 3ppm max. first year, $\pm$ 2ppm/year thereafter
Enable/Disable:	Enable high. No connection or Vdd-0.5V min. is applied to E/D pad to enable output. Ground +0.5V max. to disable output

### OUTLINE AND DIMENSIONS



### FREQUENCY STABILITY OVER TEMPERATURE

Frequency Stability over Operating Temp. Range*	$\pm$ 25ppm	$\pm$ 50ppm	$\pm$ 100ppm
Commercial -10° to +70°C	A	B	C
Industrial -40 to +85°C	D	E	F

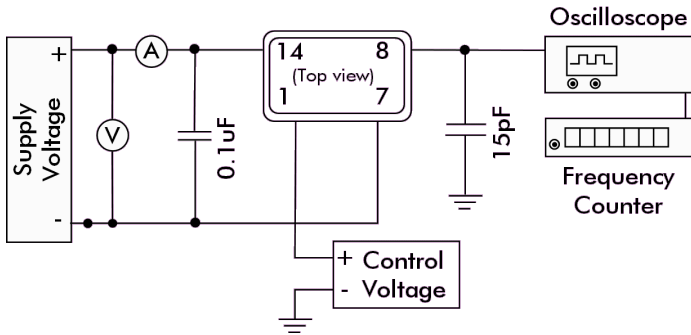
\* If non-standard temperature stability is required enter the desired stability in ppm after either 'C' (-10° to +70°) or 'I' (-40° to +85°C)  
Example: 'C20' =  $\pm$ 20ppm over -10 to +70°C

### PHASE NOISE at 156.250MHz

Offset	Value
10Hz	-62 dBc/Hz
100Hz	-92 dBc/Hz
1kHz	-120 dBc/Hz
10kHz	-132 dBc/Hz
100kHz	-128 dBc/Hz
1MHz	-140 dBc/Hz
10MHz	-150 dBc/Hz

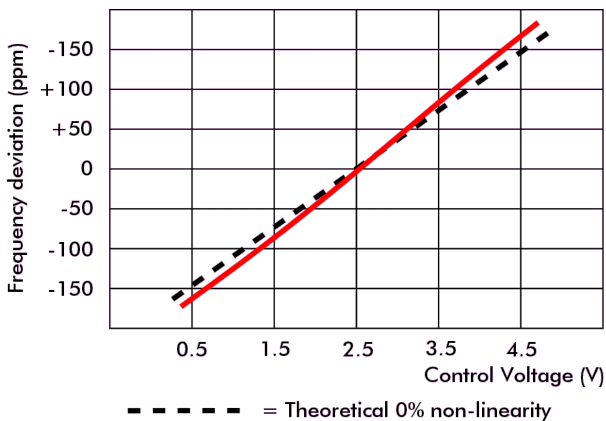
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### CMOS/TTL TEST CIRCUIT



### TRANSFER FUNCTION

Typical response of 5G14-C-150N-27.000  
(at 25°C, positive transfer)



### PART NUMBER SCHEDULE

Example: 3 GF8 B - 80 N - 156.250

Supply Voltage +3.3V

Series Designator GF8

Add 'G' here for RoHS compliance

Stability over Temperature Range

A = ±25ppm over -10° to +60°C

B = ±50ppm over -10° to +60°C

C = ±100ppm over -10° to +60°C

D = ±25ppm over -40° to +85°C

E = ±50ppm over -40° to +85°C

F = ±100ppm over -40° to +85°C

Pullability in ±ppm

Pullability Determinator

N = minimum

M = maximum

T = Typical

Frequency in MHz