# HPF576 PECL OSCILLATORS

## 7 x 5mm SMD



### FEATURES

- Industry-standard 6 pad 7.0 x 5.0mm SMD package
- Frequency Range 38.0MHz to 640.0MHz
- High Q fundamental crystal and low jitter multiplier circuit
- Supply voltage +2.5V or +3.3Volts
- Tristate function to conserve power
- Phase jitter <1ps

RoHS

### DESCRIPTION

HPF576 series oscillators provide a high quality differential PECL output at frequencies from 38.0MHz to 640.0MHz. Phase jitter <1ps. Power supply voltages may be specified as +2.5 volts or +3.3 Volts.

### SPECIFICATION

| Model: | HPF576 | |
|---|---|---|
| Output Logic: | LVPECL | |
| | 38MHz to 640MHz | |
| Supply Voltage Vdd: | +2.5VDC±5% | +3.3VDC±5% |
| Supply Voltage Code: | '25' | '3' |
| Output Logic 'HIGH', '1': | Vdd-1.025 min. Term. RL = 50Ω to Vdd-2.0V* | |
| Output Logic 'LOW', '0': | Vdd-1.625 max. Term. RL = 50Ω to Vdd-2.0V* | |
| Integrated Phase Jitter: (12kHz to 20MHz) | 0.4ps typical; 0.5ps max. for 156.250MHz | |
| Period jitter RMS: (Decoupling capacitor between Vdd and ground.) | 3ps typical, 5ps maximum for 156.250MHz | |
| Period Jitter Peak to Peak: (Decoupling capacitor between Vdd and ground.) | 20ps typical, 30ps maximum for 156.250MHz | |
| Current Consumption (15pF Load): | 38MHz to 100MHz: 65mA max.<br>100.01MHz to 320MHz: 80mA max.<br>320.01MHz to 640.0MHz: 90mA max. | |
| Rise/Fall Time: | 0.4ns typical, 0.55ns max. (20% to 80% of PECL waveform) | |

### PHASE NOISE

| Offset | Frequency 156.250MHz |
|---|---|
| 10Hz | -62 dBc/Hz |
| 100Hz | -92 dBc/Hz |
| 1kHz | -120 dBc/Hz |
| 10kHz | -132 dBc/Hz |
| 100kHz | -128 dBc/Hz |
| 1MHz | -140 dBc/Hz |
| 10MHz | -150 dBc/Hz |

### GENERAL SPECIFICATION

| | |
|---|---|
| Frequency Stability: | From ±25ppm over -40° to +85°C *(See part number table)* |
| Load: | RL = 50Ω (Vdd-2.0V)* |
| Start-up Time: | 10ms maximum |
| Duty Cycle: | 50%±5% *measured at Vdd-1.3V* |
| Storage temperature: | -55° to +150°C |
| Enable/Disable (Tristate) | |
| Enable: | No connection to tristate pad, both PECL and comp. PECL outputs enable. |
| Enable: | When disabled, both outputs are enabled when tristate pad is taken above 0.45 Vdd, ref. to ground. |
| Disable: | Both outputs are disabled when the tristate pad is taken below 0.45 Vdd. Oscillator is always on, only buffer stage is disabled. Tristate pads: type 5761 on pad 1, type 5762 on pad 2. |
| Input Static Discharge protection: | 2kV minimum. |

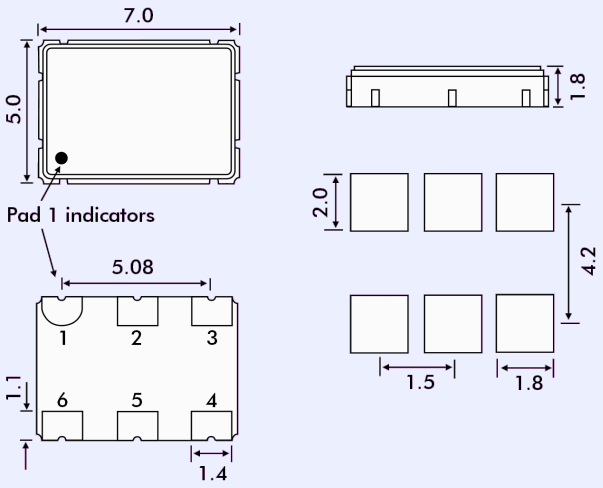
** Note: See test circuit diagram on page 2.*

### ABSOLUTE MAXIMUM RATINGS

**Permanent damage may occur if units are operated beyond specified limits.**

| | |
|---|---|
| Supply Voltage: | +4.6 VDC max. |
| Input Voltage Vi: | Vss-0.5 min., Vdd +0.5V max. |
| Input Voltage Vo: | Vss-0.5 min., Vdd +0.5V max. |

### OUTLINE & DIMENSIONS




Pad Connections HPF5761

1: Enable/Disable
2: Not connected
3: Ground
4: Output
5: Complimentary Output
6: Vcc

Pad Connections HPF5762

1: Not connected
2: Enable/Disable
3: Ground
4: Output
5: Complimentary Output
6: Vcc

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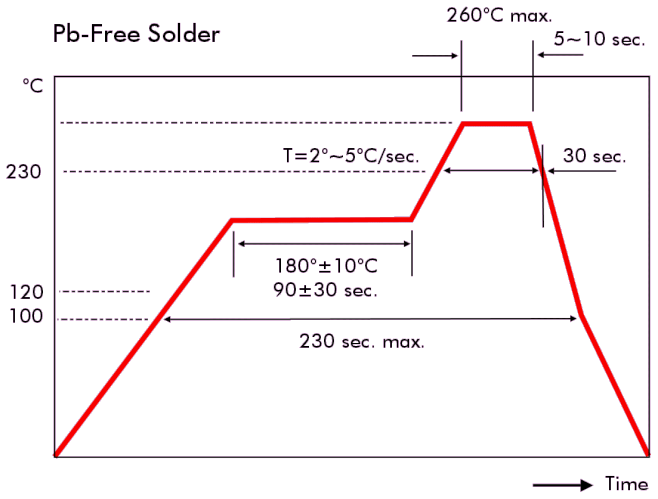
## SOLDER PROFILE




## PART NUMBER FORMAT

Example 3HPF5761-DT-156.52

3HPF5761- D T - 156.52

Supply Voltage:
3 = 3.3 Volts

Package Designation*:
HPF5761
HPF5762

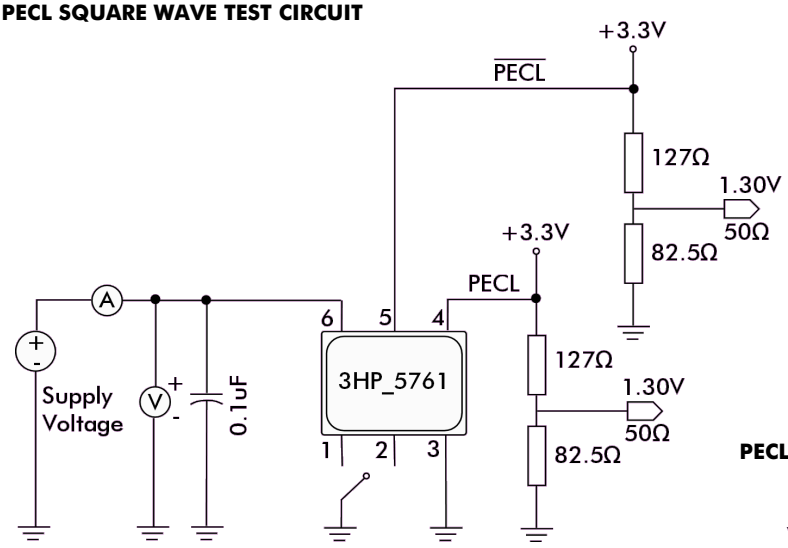
Stability over Temperature Range:
A = ±25ppm over -10° to +70°C
B = ±50ppm over -10° to +70°C
C = ±100ppm over -10° to +70°C
D = ±25ppm over -40° to +85°C
E = ±50ppm over -40° to +85°C
F = ±100ppm over -40° to +85°C

Tristate (Enable/Disable) Function

Nominal Frequency (MHz):

** Package Variants:*
*HPF5761 = Tristate (enable/disable) on Pad 1.*
*HPF5762 = Tristate (enable/disable) on Pad 2.*
*Check with Mercury sales office for availability.*

## PECL SQUARE WAVE TEST CIRCUIT




## PECL SQUARE WAVE WAVEFORM