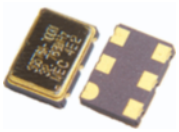
HDF5761 LVDS OSCILLATORS

7 x 5 x 1.4mm SMD

FEATURES

- Industry-standard 6 pad 7.0 x 5.0mm SMD package
- Frequency Range 38MHz to 640.0MHz
- High Q fundamental mode crystal with low jitter multiplier circuit
- Supply voltage +2.5V or +3.3Volts
- Tristate function to conserve power
- Phase jitter <1ps



DESCRIPTION

HDF5761 series oscillators provide a high quality LVDS output at frequencies from 38MHz to 640.0MHz. Phase jitter <0.5ps. Power supply voltages may be specified as +2.5 Volts or +3.3 Volts.

SPECIFICATION

Model:	HDF5761	
Output Logic:	LVDS	
Frequency Range:	38MHz to 640.0MHz	
Supply Voltage Vdd:	+2.5VDC±5%	+3.3VDC±5%
Supply Voltage Code:	'25'	'3'
Output Logic 'HIGH', '1':	1.4 Volts typical, 1.6 Volts maximum*	
Output Logic 'LOW', '0':	0.9 Volts minimum, 1.1 Volts*	
Differential Output Voltage (Vod):	247mV min., 355mV typ., 454mV max. O/p1-O/p2	
Differential Output Error (dVod):	-50mV minimum, 50mV max.	
Output Offset Voltage (Vos):	1.125V min., 1.200 V typical, 1.375V max.	
Offset Magnitude Error (dVos):	0mV min. 3mV typical, 25mV max.	
Integrated Phase Jitter: (12kHz to 20MHz)	0.4ps typical; 0.5ps max. for 156.250MHz	
Period jitter RMS**:	3ps typical, 5ps maximum for 156.250MHz	
Period Jitter Peak to Peak**:	20ps typical for 156.250MHz	
Current Consumption (15pF Load):	*See table*	
Rise/Fall Time:	0.4ns typical, 0.7ns max. (20% to 80% of LVDS waveform)	

***Note: Measured with decoupling capacitor between Vdd and Ground.*

PHASE NOISE

Offset	Frequency 156.250MHz
10Hz	-62 dBc/Hz
100Hz	-92 dBc/Hz
1kHz	-120 dBc/Hz
10kHz	-132 dBc/Hz
100kHz	-128 dBc/Hz
1MHz	-140 dBc/Hz
10MHz	-150 dBc/Hz

CURRENT CONSUMPTION

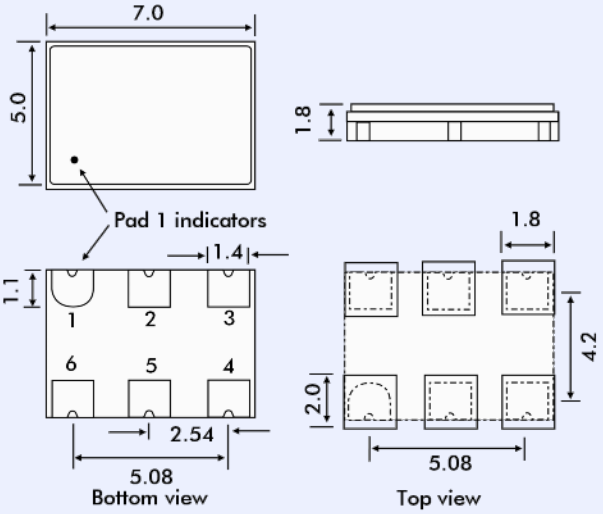
Frequency	Current
38MHz ~ 100MHz	65mA max.
100.01MHz ~ 320MHz	85mA max.
320.01Mhz ~ 640MHz	90mA max.

GENERAL SPECIFICATION

Frequency Stability:	From ±25ppm over -40° to +85°C *(See part number table)*
Load:	50Ω from each output
Start-up Time:	5ms typical, 10ms maximum
Duty Cycle:	50%±5% *measured at 1.25 Volts*
Drive Capability:	100Ω between LVDS and comp. LVDS
Storage temperature:	-55° to +150°C
Enable/Disable (Tristate)	
Enable:	No connection to tristate pad, both LVDS and comp. LVDS outputs enable.
Enable:	When disabled, both outputs are enabled when tristate pad is taken above 0.45 Vdd, ref. to ground.
Disable:	Both outputs are disabled when the tristate pad is taken below 0.45 Vdd. Oscillator is always on, only buffer stage is disabled. Tristate pads: type 5761 on pad 1, type 5762 on pad 2.
Input Static Discharge protection: 2kV minimum.	
Ageing:	±3ppm max., first year, ±2ppm max. per year thereafter

** Note: See test circuit diagram on page 2.*

OUTLINE & DIMENSIONS



Pad Connections HDF5761
1 Tristate
2 No Connection
3 Ground
4 LVDS Output
5 Complimentary Output
6 Supply Voltage

ABSOLUTE MAXIMUM RATINGS

Permanent damage may occur if units are operated beyond specified limits.

Supply Voltage:	+4.6 VDC max.
Input Voltage Vss:	Vss-0.5 min., Vdd +0.5V max.
Input Voltage Vss:	Vss-0.5 min., Vdd +0.5V max.

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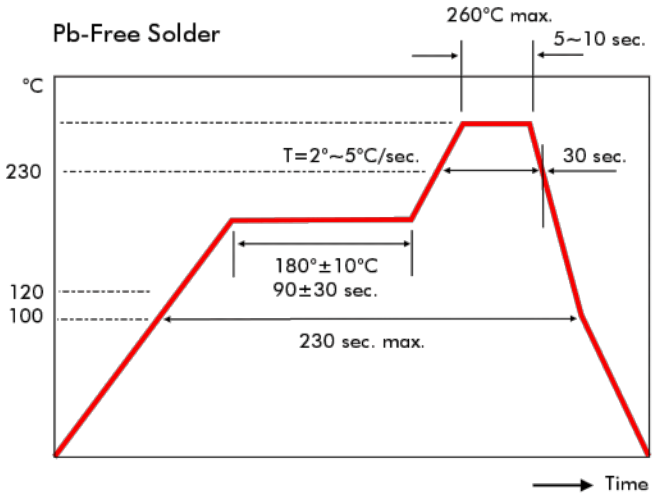
SOLDER PROFILE



PART NUMBER FORMAT

Example 3HDF5761-DT-156.52

3HDF5761- D T - 156.52

Supply Voltage:
3 = +3.3 Volts
25 = +2.5 Volts

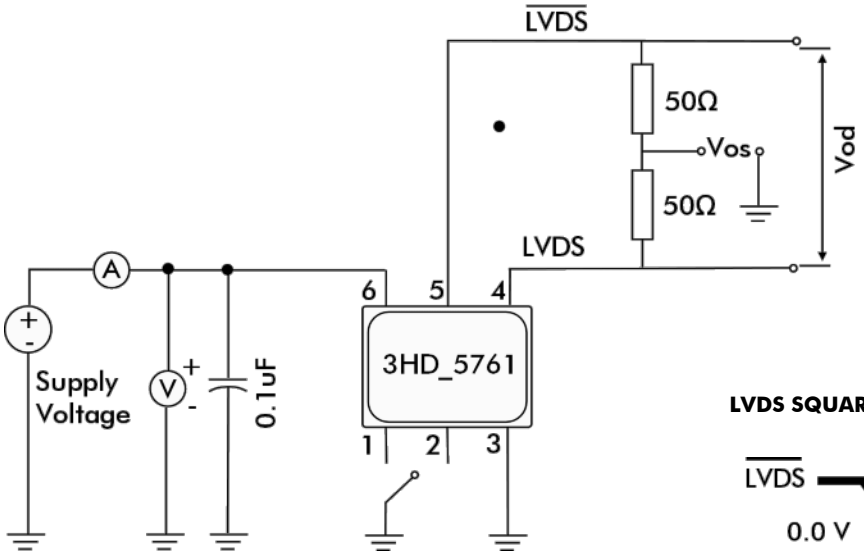
Series Designation:
HDF5761

Stability over Temperature Range:
A = ±25ppm over -10° to +70°C
B = ±50ppm over -10° to +70°C
C = ±100ppm over -10° to +70°C
D = ±25ppm over -40° to +85°C
E = ±50ppm over -40° to +85°C
F = ±100ppm over -40° to +85°C

Tristate (Enable/Disable) Function

Nominal Frequency (MHz):

LVDS SQUARE WAVE TEST CIRCUIT



LVDS SQUARE WAVE WAVEFORM