

M2075/M2076 Series SPECIFICATION FOR 5.0x7.0mm LVPECL/LVDS SMT OSCILLATOR

FEATURES

LVPECL/LVDS Differential Output
RMS Phase Jitter < 700 fs, 12 kHz to 20 MHz
(156.25 MHz, PECL output)
Low Phase Noise
3rd Overtone crystal technology
Compliant to RoHS directive

APPLICATIONS

10 Gigabit Ethernet switches/routers
Network Interface

Ordering Information:

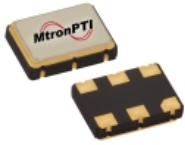
Product Family (Supply Voltage Option)	Temperature Range		Stability *		Enable/Disable		Logic Type		Package/Lead Configuration		Frequency
	Code	Value	Code	Value	Code	Value	Code	Value	Code	Value	
M2075 (3.3V)	1	0 °C to +70 °C	3	±100 ppm	B	Enable High (pad 1)	P	LVPECL LVDS	N	Leadless	XXX.XXXX MHz
	2	-40 °C to +85 °C	4	±50 ppm	G	Enable High (pad 2)					
M2076 (2.5V)	6	-20 °C to +70 °C	6	±25 ppm	U	No Enable/Disable					
	7	0 °C to +85 °C	8	±20 ppm							
Example: M207524BPN 156.2500 MHz											
M2075	2		4		B		P		N		156.2500 MHz

* Stability includes initial tolerance @ +25°C, deviation over operating temperature, variations to supply voltage, load, vibration and shock.

LVPECL Electrical Specifications:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Frequency of Operation	F _O	25		320	MHz	
Frequency Stability						
Frequency Stability	ΔF/F	See ordering information				
Aging		-5		+5	ppm	1 st year
RF Output						
Output Type		LVPECL Compatible				
Output Load		50 Ω to (V _{CC} -2.0) V _{DC}				V
Symmetry (duty cycle)	V _{OH}	45		55	%	Ref. to 50% of waveform
Logic Level "1"	V _{OH}	V _{CC} -1.025			V	0 to +85 °C
	V _{OH}	V _{CC} -1.085			V	-40 to 0 °C
Logic Level "0"	V _{OL}			V _{CC} -1.620	V	0 to +85 °C
	V _{OL}			V _{CC} -1.550	V	-40 to 0 °C
Rise/Fall Time	T _R /T _F		0.3	0.5	ns	20% to 80% of waveform
Start-up Time	T _{SU}			10	ms	T _{ambient} = +25°C
Enable Logic		70% V _{CC} or N/C			V	Pad 1 or Pad 2: Output Enabled
Disable Logic				30% V _{CC}	V	Pad 1 or Pad 2: Output Disabled to high-Z
Supply Voltage & Power Consumption						
Operating Voltage	V _{CC}	3.135	3.300	3.465	V	
Supply Current	I _{CC}			100	mA	
Other Parameters						
Phase Jitter (RMS)	Φ _J			0.700	ps	12 KHz to 20 MHz 156.25 MHz

Revision
06/02/15



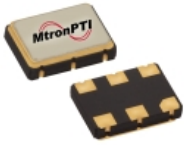
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LVDS Electrical Specifications:

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	
Frequency of Operation	F_O	25		320	MHz		
Frequency Stability							
Frequency Stability	$\Delta F/F$	See ordering information					
Aging		-5		+5	ppm	1 st year	
RF Output							
Output Type		LVDS Compatible					
Output Load		100 Ω Differential			V		
Symmetry (duty cycle)	V_{OH}	45		55	%	Ref. to 50% of waveform peak-to-peak differential output voltage	
Differential Output Voltage	V_{DIFF}	250	350	450	mV		
Output Offset Voltage	V_{OS}	1.125	1.250	1.375	V		
Rise/Fall Time	T_R/T_F		0.3	0.5	ns	20% to 80% of waveform	
Start-up Time	T_{SU}			10	ms	$T_{ambient} = +25^\circ C$	
Enable Logic		70% V_{CC} or N/C			V	Pad 1 or Pad 2: Output Enabled	
Disable Logic				30% V_{CC}	V	Pad 1 or Pad 2: Output Disabled to high-Z	
Supply Voltage & Power Consumption							
Operating Voltage	V_{CC}	3.135	3.300	3.465	V		
Supply Current	I_{CC}			60	mA		
Other Parameters							
Phase Jitter (RMS)	Φ_J			0.700	ps	12 KHz to 20 MHz 156.25 MHz	

Environmental & Packaging Requirements:

Storage Temperature	-55°C to 125 °C
Mechanical Shock	Per MIL-STD-202, Method 213, Condition C (100 g's, 6 ms)
Vibration	Per MIL-STD-202, Method 204, Condition C (55 – 2000 Hz, 10 g's)
Aging	+85°C \pm 3°C, 720H (No BIAS)
Humidity	+40°C \pm 2°C X90~95%, 96H (NO BIAS)
Thermal Cycle	Per MIL-STD-883, Method 1010, Condition B (-55 to +125 °C, 10 cycles)
Hermeticity	Per MIL-STD-202, Method 112 (1 x 10 ⁻⁸ atm cc/s of Helium)
Moisture Sensitivity Level	MSL1
Solderability	Per EIAJ-STD-002, Method 208
Max. Soldering Conditions	See solder profile, Figure 1
Pad Termination	Gold, 1 μ m maximum thickness
Package Type	6-pad 5.0 X 7.0 mm leadless ceramic. RoHS compliant.



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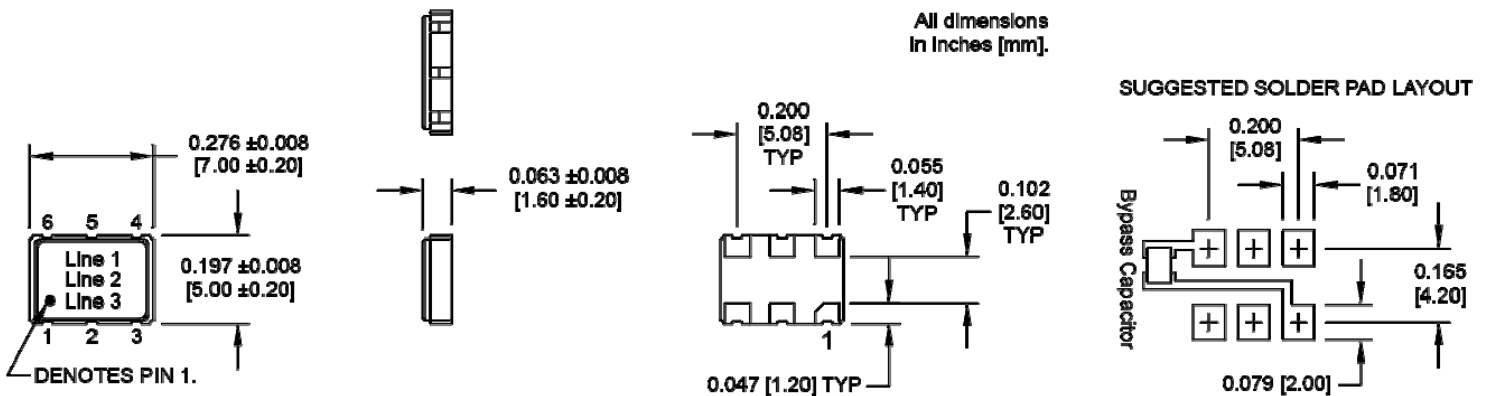
Marking, Pin Out:

Pad	Function
1	Enable/Disable or N/C
2	Enable/Disable or N/C
3	Ground
4	Output
5	Complementary Output
6	+V _{CC}

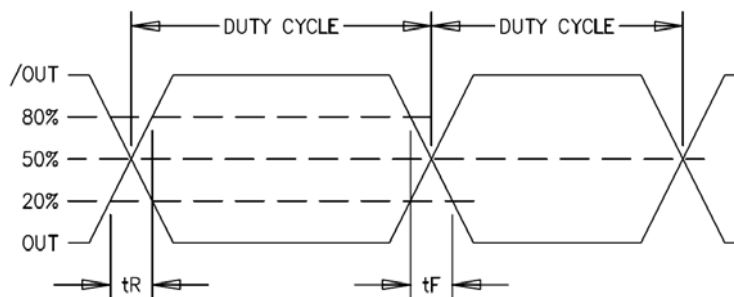
Part Marking	
Line 1	[part designation]
Line 2	FFFMFFFF
Line 3	M yy ww vv

Legend	
M	MtronPTI
F	Frequency
yy	Year
ww	Work Week
vv	Factory code

Dimensions:



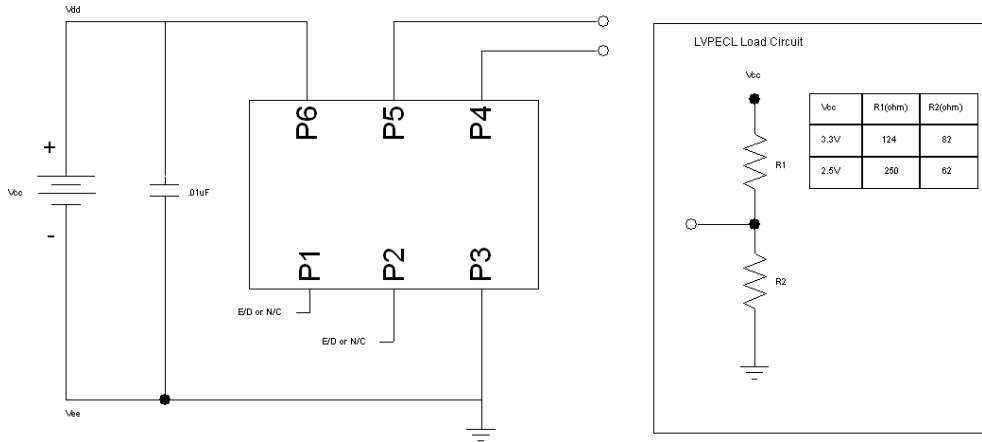
Output Waveform:



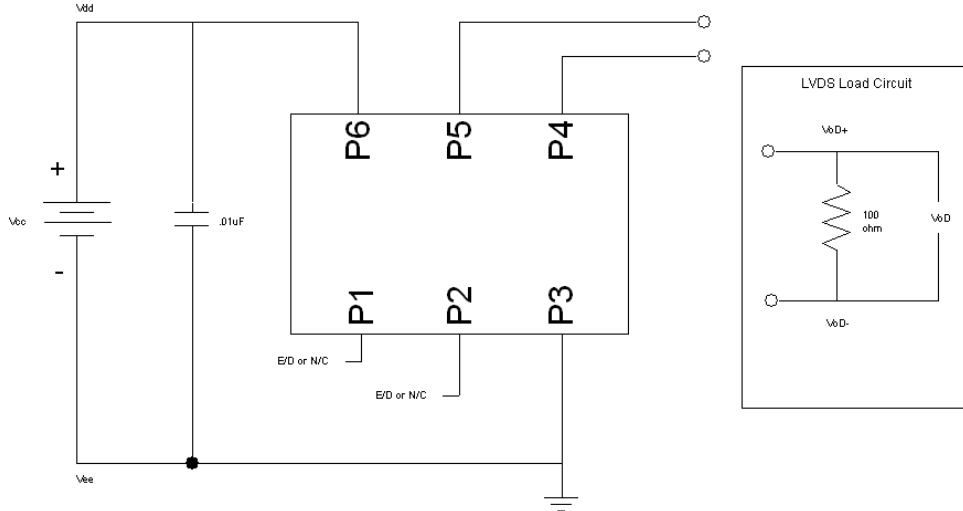


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Typical LVPECL Test Circuit & Load Circuit Diagrams:



Typical LVDS Test Circuit & Load Circuit Diagrams:





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Soldering Conditions:

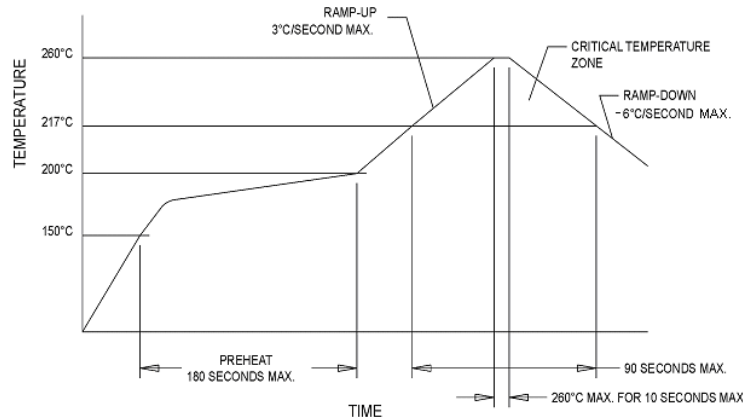
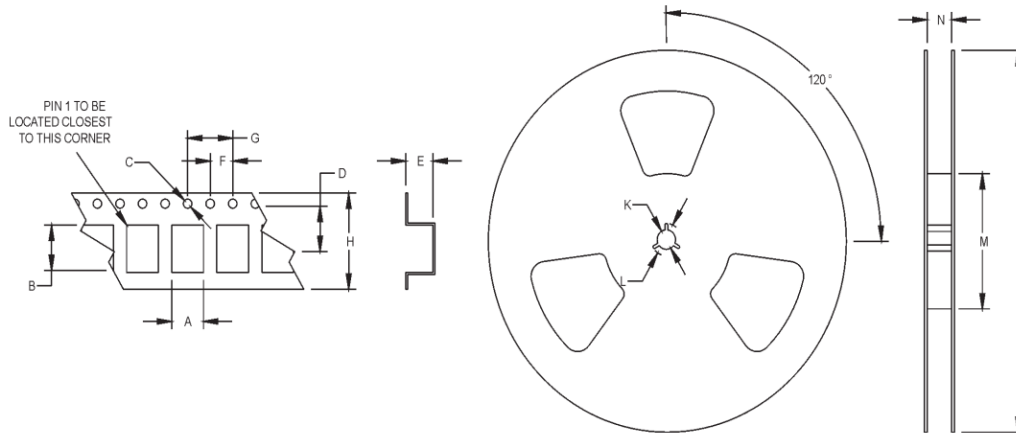


Figure 1

Tape and Reel Specifications:

All units in mm



Tape and Reel Specifications											
A	B	C	D	E	F	G	H	J	K	L	M
5.32	7.28	1.5	7.5	2.2	4	8	16	178	13.5	24.8	80