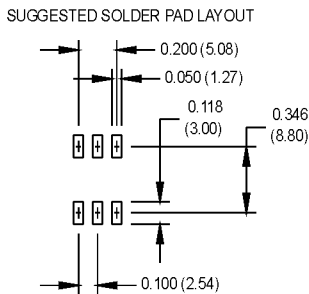
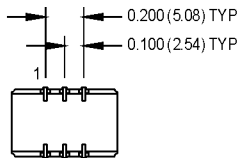
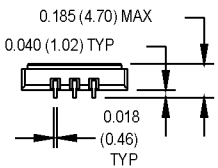
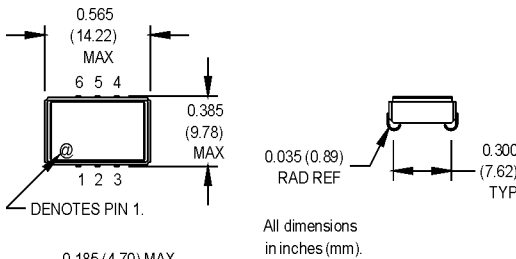


# MPV3 Series

## 9x14 mm, 3.3 Volt, LVPECL/LVDS, VCXO



- Versatile VCXO to 800 MHz with good jitter (3 ps typical)
- Used in low jitter clock synthesizers and SONET applications



### Pin Connections

PIN	FUNCTION
1	Control Voltage
2	Enable/Disable or N/C
3	Ground/Case
4	Output Q
5	Output $\bar{Q}$ or N/C
6	+Vcc

### Ordering Information

Product Series	MPV3	1	0	R	1	L	J	-R	00.0000 MHz
Temperature Range	1: 0°C to +70°C    2: -40°C to +85°C 6: -20°C to +70°C    8: 0°C to +50°C								
Stability	0: Nominal per APR selection 1: ±50 ppm (±35 ppm typ. Stability) 2: ±100 ppm (±20 ppm typ. Stability) 5: ±80 ppm (±25 ppm typ. Stability) 8: ±25 ppm (±50 ppm typ. Stability)								
Output Type	R: Complementary, Enable Z: Complementary, w/o Enable								
Absolute Pull Range	L: 45/55% LVDS    P: 45/55% PECL H: 40/60% LVDS    Q: 40/60% PECL								
Symmetry/Output Logic Type	J: J-lead RoHS Compliance Blank: non-RoHS compliant part -R: RoHS compliant part Frequency (customer specified)								

PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes	
Frequency Range	F	0.75		800	MHz		
Operating Temperature	T <sub>A</sub>	(See Ordering Information)					
Storage Temperature	T <sub>S</sub>	-55		+125	°C		
Frequency Stability	ΔF/F	(See Ordering Information)					See Note 1
Aging							
1st Year		-3/-5		+3/+5	ppm	< 52 MHz / ≥ 52 MHz	
Thereafter (per year)		-1/-2		+1/+2	ppm	< 52 MHz / ≥ 52 MHz	
Pullability/APR		(See Ordering Information)					See Note 2
Control Voltage	V <sub>c</sub>	0.3	1.65	3	V	Pin 1 voltage	
Linearity			5	10	%	Positive Monotonic Slope	
Modulation Bandwidth	f <sub>m</sub>	10			kHz	-3 dB bandwidth	
Input Impedance	Z <sub>in</sub>	50k			Ohms		
Input Voltage	V <sub>cc</sub>	3.135	3.3	3.465	V		
Input Current	I <sub>cc</sub>						
0.75 MHz to 26 MHz				60/30	mA	PECL/LVDS	
26 MHz to 104 MHz				95/60	mA	PECL/LVDS	
104 MHz to 800 MHz				105/60	mA	PECL/LVDS	
Output Type						PECL/LVDS	
Load		50 Ohms to V <sub>cc</sub> -2 VDC				See Note 3	
		100 Ohm differential load				PECL waveform LVDS waveform	
Symmetry (Duty Cycle) (Per Symmetry Code)		(See Ordering Information)					V <sub>cc</sub> -1.3 VDC (PECL) 50% of Waveform (LVDS)
Output Skew				200	ps		
Differential Voltage	V <sub>o</sub>	250	340	450	mV	LVDS only	
Logic "1" Level	V <sub>oh</sub>	V <sub>cc</sub> -1.02			V	PECL	
Logic "0" Level	V <sub>ol</sub>	V <sub>cc</sub> -1.63			V	PECL	
Rise/Fall Time	T <sub>r</sub> /T <sub>f</sub>		0.35	0.55	ns	@ 20/80% LVPECL	
			.50	1.0	ns	@ 20/80% LVDS	
Enable Function		80% V <sub>cc</sub> min or N/C: output active 20% V <sub>cc</sub> max: output disables to high-Z					
Start up Time		5			ps		
Phase Jitter	φ <sub>J</sub>		3	5	ps RMS	Integrated 12 kHz - 20 MHz	
Phase Noise (Typical)						Offset from carrier	
@ 19.44 MHz		-60	-90	-112	-140	-150	dBc/Hz
@ 155.52 MHz		-60	-90	-112	-123	-120	dBc/Hz
@ 622.08 MHz		-60	-90	-108	-108	-105	dBc/Hz

- Stability given for deviation over temperature.
- APR specification inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging.
- PECL load - see load circuit diagram #5. LVDS load - see load circuit diagram #9.

MtronPTI reserves the right to make changes to the product(s) and service(s) described herein without notice. No liability is assumed as a result of their use or application.

Please see [www.mtronpti.com](http://www.mtronpti.com) for our complete offering and detailed datasheets. Contact us for your application specific requirements: MtronPTI 1-800-762-8800.

# MtronPTI Lead Free Solder Profile

