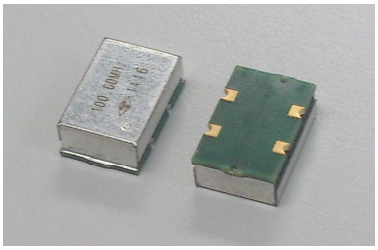
High Frequency Very Low Noise VCXO
VLCU-Type series

VLCU-Type Series in 14 x 9mm SMD package

VLCU-Type series is a high frequency high performance VCXO offering high frequency and very low phase noise. The part comes in a small SMD package which makes it suitable for reflow soldering during pick and place assembly.



RoHS Compliant Standard

FEATURES

- **Low Phase Noise**
- Small SMD Package
- Low Power Consumption

APPLICATIONS

- Instrument
- Microwave Communication
- Test & Measurement
- Telecom Systems
- Satellite Communication

ELECTRICAL SPECIFICATIONS

1. OUTPUT (PIN = "R.F. OUTPUT")

	Parameter	Min.	Typ.	Max.	Unit	Test Condition
1.1.	Frequency (Fo)	50		125	MHz	Standard Frequency : 100MHz, 122.88MHz, 125MHz
1.2.	Frequency Stability (Overall)	-35		+35	ppm	Frequency stability includes frequency tolerance@25℃ and frequency stability vs. operating temperature range and voltage variance and 15 years aging.
1.3.	Operating Temperature Range	-20°C ~ +70°C -40°C ~ +85°C			°C	
1.4.	Storage Temperature Range	-45°C ~ +90°C			°C	
1.5.	Waveform	Sine wave				
1.6.	Level	+8			dBm	
1.7.	Load		50		Ω	
1.8.	Harmonics			-22	dBc	
1.1.	Phase Noise (Max.) (Fo =100MHz)	Option A	Option B	Option C		
1.2.		-84	-87	-90	dBc/Hz	@ 10Hz
1.3.		-117	-120	-123	dBc/Hz	@ 100Hz
1.4.		-143	-144	-145	dBc/Hz	@ 1KHz
1.5.		-165	-165	-165	dBc/Hz	@ 10KHz
1.6.		-170	-170	-170	dBc/Hz	@ 100KHz
1.7.		-172	-172	-172	dBc/Hz	@ 1MHz

2. ELECTRICAL FREQUENCY ADJUSTMENT (PIN = "VCO INPUT")

	Parameter	Min.	Typ.	Max.	Unit	Test Condition
2.1.	Pulling Range	+/-35			ppm	
2.2.	Control Voltage	0		+5.0	V	
2.3.	Slope		Positive			
2.4.	Center Voltage		+2.5		V	
2.5.	Linearity	-10		+10	%	
2.6.	Modulation Bandwidth	5			KHz	
2.7.	VC Input Impedance	1			Mohm	

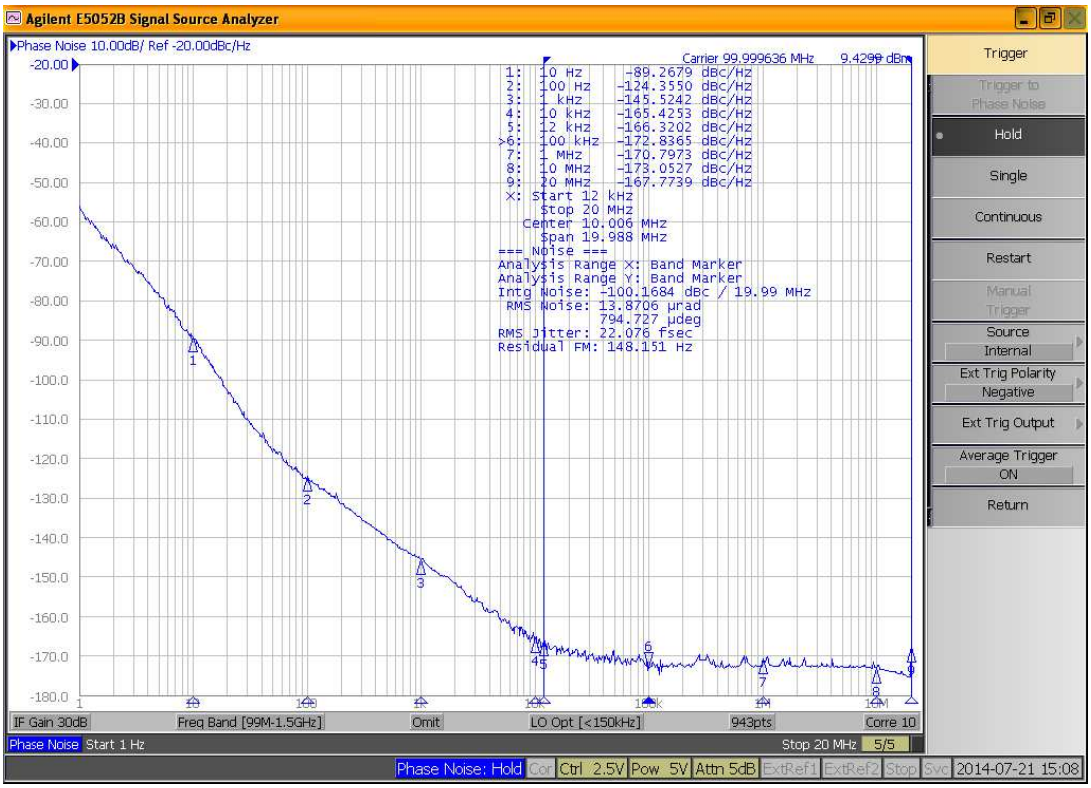
3. INPUT POWER (PIN = "+VDC")

	Parameter	Min.	Typ.	Max.	Unit	Test Condition
3.1.	Voltage	+4.75	+5	+5.25	V	
3.2.	Current			30	mA	At maximum supply voltage

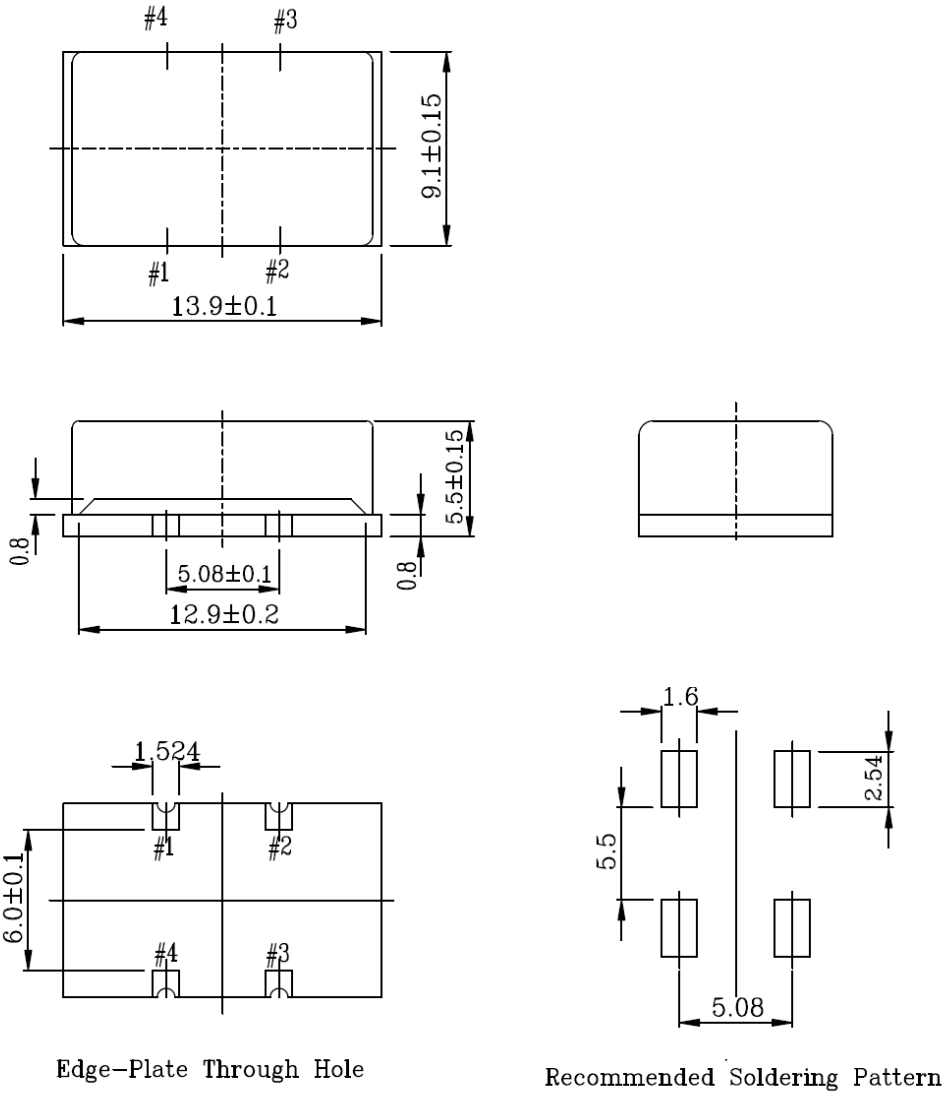
4. ENVIRONMENTAL

	Parameter	Reference Std.	Test Condition
4.1.	Vibration Test	DIN EN 60068-2-6	10~55Hz, 0.75mm Peak; 55~2000Hz, 10g Peak. 10 Cycles; 3 axis; 1Oct./min.
4.2.	Thermal Shock	DIN EN 60068-2-14	30 min. @each temperature 10 cycles, Transfer<1min.; -40℃+/-3℃; 85℃+/-3℃
4.3.	Mechanical Shock	DIN EN 60068-2-27	6 shocks per axis, 100g; 6ms both directions

PHASE NOISE TEST DATA



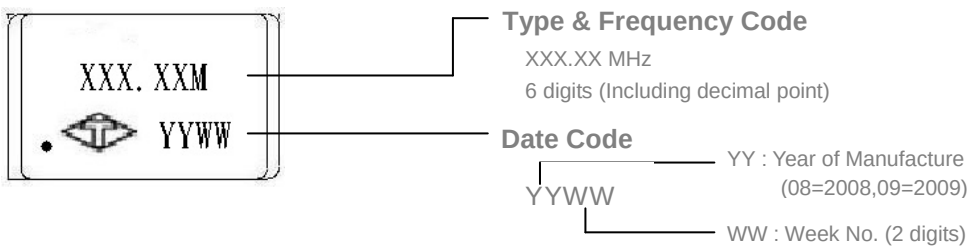
OUTLINE DRAWING



Pin FUNCTIONS

Pin	Function
#1	Vcon
#2	GND
#3	Output
#4	VDD

PRODUCT IDENTIFICATION (MARKING)



Model Numbering Guide – VCXO

Available options

Type	package (mm)	Supply Voltage(V)	Tri-State Function	Freq.Stability/ APR (ppm)	Temp. Range(°C)	Output Logic and Symmetry	Oscillator Mode	Appearance	Lead Free	Dash	Freq. (MHz)
V: VCXO	W: 5.0x3.2 (6 Pads) T: 7.0x5.0 (6 Pads) K: 14.2x9.3 (6 Pads) L: 14.0x9.0 (4 Pads)	C: 5 (Only for L Package) E: 3.3 J:2.5 K: 1.8 (Only for CMOS and Frequency < 60MHz)	U: Relative Pulling (Refer to Center Voltage) with Tri-State to pin 2 M: Multiplier Frequency with Tri-State to pin 2 S: Enable Low R: Input to pin 5 F: Without Tri-State	M: ±25/±50 (VC=10%Vdd ~90%Vdd) P: ±50/±50 (VC=10%Vdd ~90%Vdd) A: ±50/±50 (VC=0V~Vdd) B: ±25/±50 (VC=0V~Vdd) V: Overall: ±35ppm Pulling: ±35ppm	I: -10~+60 C: -20~+70 L: -40~+85 J:-40~+105	J: CMOS 15pF / 50±5% F: CMOS 50pF / 50±5% L: LVPECL / 50±5% V: LVDS / 50±5% W: Sine Wave	A: AT Fundamental T: AT 3rd Overtone Not selectable by Customer	N: Normal F: Option A G: Option B J: Option C	F: RoHs Compliant	–	XX.XXXXXX

V T E S P C L A N F – 10.000000

*Not all combinations of options are available.

Example: VTESPCLANF-10.000000

Type	VCXO
Package	7.0 x 5.0 mm
Supply Voltage(V)	3.3 V
Tri-State	Enable Low
Freq. Stability / APR	±50ppm / ±50ppm
Temp Range	-20~+70 °C
Output	LVPECL/Symmetry 50±5%
Oscillator Mode	AT Fundamental
Appearance	Normal Appearance
Lead Free	RoHs Compliant
Frequency	10.000000 MHz