

# VW Type

## 5.0 x 3.2mm SMD Voltage Controlled Crystal Oscillator

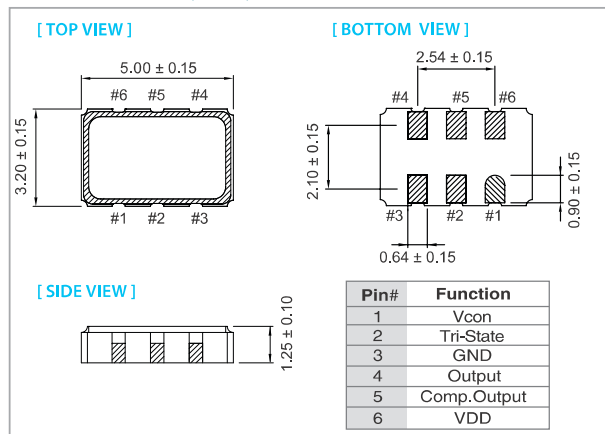
### FEATURE

- Typical 5.0 x 3.2 x 1.25 mm 6 pads ceramic SMD package.
- Tight symmetry (45 to 55%) available.
- Operating temperature up to 105°C
- Tri-state enable/disable

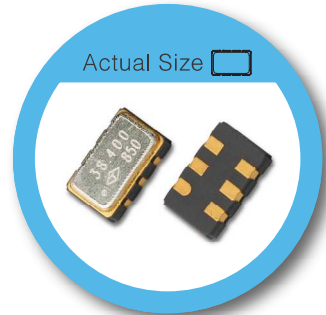
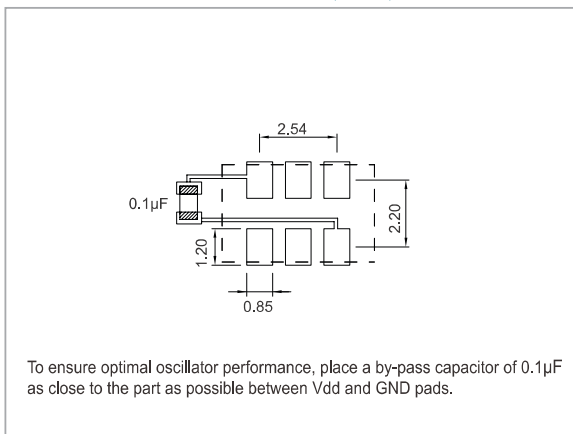
### TYPICAL APPLICATION

- Set-top Box, HDTV
- WiMAX/WLAN
- xDSL/ VoIP, Cable modem

### DIMENSION (mm)



### SOLDER PAD LAYOUT (mm)



RoHS Compliant

### ELECTRICAL SPECIFICATION

Parameter	3.3V		Unit
	Min	Max.	
Supply Voltage Variation (VDD)	VDD-5%	VDD+5%	V
Frequency Range	1.5	170	MHz
Standard Frequency	19.44, 38.4		
Absolute Pulling Range (APR)	±50	-	ppm
Control Voltage Range	0.3	3.0	V
Supply Current	1.5 MHz ≤ Fo < 20 MHz	-	10
	20 MHz ≤ Fo < 50 MHz	-	20
	50 MHz ≤ Fo ≤ 170 MHz	-	30
Output Level	Output High (Logic"1")	2.97	-
	Output Low (Logic"0")	-	0.33
Transition Time: Rise/Fall Time+	1.5 MHz ≤ Fo < 20 MHz	-	5
	20 MHz ≤ Fo < 50 MHz	-	4
	50 MHz ≤ Fo ≤ 170 MHz	-	3
Start Time	-	2	mSec
Tri-State (input to Pin 2)	Enable (High voltage or floating)	2.31	-
	Disable (Low voltage or GND)	-	0.99
Linearity	-	10	%
Modulation Bandwidth (BW)	1.5 MHz ≤ Fo ≤ 170 MHz	15	-
Input Impedance	10000	-	kΩ
Period Jitter (Pk-Pk)	-	40	pSec
RMS Phase Jitter (Integrated 12 kHz ~ 20 MHz)	-	1	pSec
Phase Noise@38.4 MHz	100 Hz	-100	
	1 kHz	-133	
	10 kHz	-140	
Aging (@ 25°C 1st year)	-	±3	ppm
Storage Temp. Range	-55	125	°C

Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.

+ Transition times are measured between 10% and 90% of VDD, with an output load of 15pF.

### FREQ. STABILITY vs. TEMP. RANGE

Temp. (°C)	ppm	
	±25	±50
-10 ~ +60	○	○
-20 ~ +70	○	○
-40 ~ +85	×	○
-40 ~ +105	×	○

\* ○: Available △: Conditional X: Not available

\* Inclusive of calibration @ 25 °C, operating temperature range, input voltage variation, load variation, aging (1<sup>st</sup> year), shock, and vibration

**Note: not all combination of options are available. Other specifications may be available upon request.**

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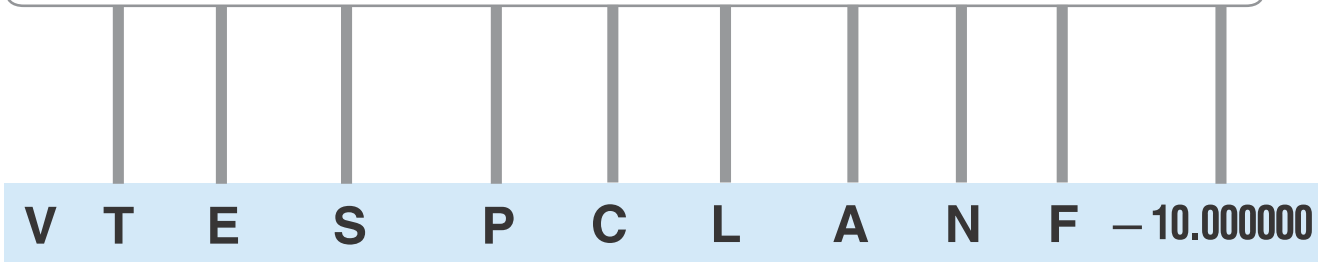
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# Model Numbering Guide – VCXO

## Available options

Type	package (mm)	Supply Voltage(V)	Tri-State Function	Freq.Stability/ APR (ppm)	Temp. Range(°C)	Output Logic and Symmetry	Oscillator Mode	Appearance	Lead Free	Dash	Freq. (MHz)
V: VCXO	W: 5.0x3.2 (6 Pads) T: 7.0x5.0 (6 Pads) K: 14.2x9.3 (6 Pads) L: 14.0x9.0 (4 Pads)	C: 5 (Only for L Package) E: 3.3 J: 2.5 K: 1.8 (Only for CMOS and Frequency < 60MHz)	U: Relative Pulling (Refer to Center Voltage) with Tri-State to pin 2 M: Multiplier Frequency with Tri-State to pin 2 S: Enable Low R: Input to pin 5 F: Without Tri-State	M: ±25/±50 (VC=10%Vdd ~90%Vdd) P: ±50/±50 (VC=10%Vdd ~90%Vdd) A: ±50/±50 (VC=0V~Vdd) B: ±25/±50 (VC=0V~Vdd) V: Overall: ±35ppm Pulling: ±35ppm	I: -10~+60 C: -20~+70 L: -40~+85 J: -40~+105	J: CMOS 15pF / 50±5% F: CMOS 50pF / 50±5% L: LVPECL / 50±5% V: LVDS / 50±5% W: Sine Wave	A: AT Fundamental T: AT 3 <sup>rd</sup> Overtone Not selectable by Customer	N: Normal F: Option A G: Option B J: Option C	F: RoHs Compliant	-	XX.XXXXXX



\*Not all combinations of options are available.

### Example: VTESPCLANF-10.000000

Type	VCXO
Package	7.0 x 5.0 mm
Supply Voltage(V)	3.3 V
Tri-State	Enable Low
Freq. Stability / APR	±50ppm / ±50ppm
Temp Range	-20~+70 °C
Output	LVPECL/Symmetry 50±5%
Oscillator Mode	AT Fundamental
Appearance	Normal Appearance
Lead Free	RoHs Compliant
Frequency	10.000000 MHz