

VW Type

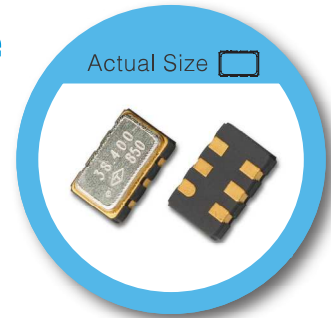
5.0 x 3.2mm SMD LVPECL/LVDS Voltage Controlled Crystal Oscillator

FEATURE

- Typical 5.0 x 3.2 x 1.25 mm 6 pads ceramic SMD package.
- Tight symmetry (45 to 55%) available.
- Tri-state enable/disable

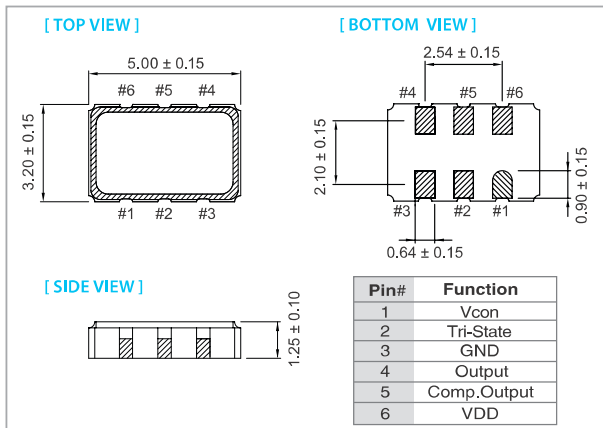
TYPICAL APPLICATION

- Set-top Box, HDTV
- WiMAX/WLAN
- xDSL/ VoIP, Cable modem

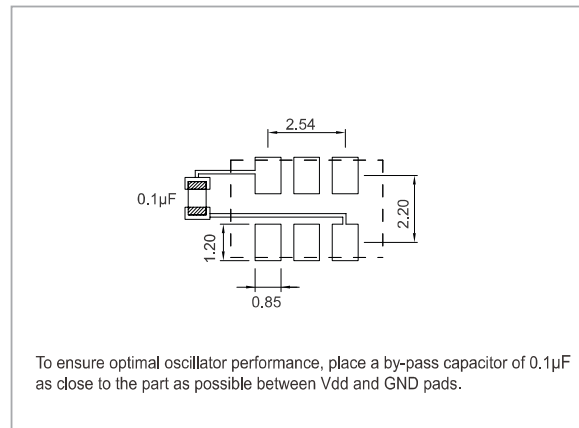


RoHS Compliant

DIMENSION (mm)



SOLDER PAD LAYOUT (mm)



ELECTRICAL SPECIFICATION

Parameter	LVPECL		LVDS		unit
	3.3 V		3.3 V		
	Min.	Max.	Min.	Max.	
Supply Voltage Variation (VDD)	VDD-5%	VDD+5%	VDD-5%	VDD+5%	V
Frequency Range	30	250	30	250	MHz
Standard Frequency	122.88, 153.6, 155.52, 156.25				
Absolute Pulling Range (APR)	±50	—	±50	—	ppm
Control Voltage Range	0.3	3.0	0.3	3.0	V
Supply Current 30 MHz ≤ Fo ≤ 250 MHz	—	100	—	75	mA
Output Level					
Output High (Logic "1")	2.275	—	—	1.6	V
Output Low (Logic "0")	—	1.68	0.9	—	
Transition Time: Rise/Fall Time*	—	1.0	—	1.0	nSec
Start Time	—	3	—	3	mSec
Tri-State (input to Pin 2)					
Enable (High voltage or floating)	2.31	—	2.31	—	V
Disable (Low voltage or GND)	—	0.99	—	0.99	
Linearity	—	10	—	10	%
Modulation Bandwidth (BW)	20	—	20	—	kHz
Input Impedance	10000	—	10000	—	KΩ
RMS Phase Jitter					
Fo < 100 MHz	—	1.0	—	1.0	pSec
100 MHz ≤ Fo < 125 MHz	—	0.7	—	0.7	
125 MHz ≤ Fo < 150 MHz	—	0.5	—	0.5	
150 MHz ≤ Fo ≤ 250 MHz	—	0.3	—	0.3	
Phase Noise@122.88MHz					dBc/Hz
100 Hz	—	-105	—	-105	
1 KHz	—	-128	—	-128	
10 KHz	—	-145	—	-145	
Aging (@ 25°C 1st year)	—	±3	—	±3	ppm
Storage Temp. Range	-55	125	-55	125	°C

Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position.

+ Transition times are measured between 20% and 80% of VDD.

FREQ. STABILITY vs. TEMP. RANGE

Temp. (°C)	ppm	
	±25	±50
-10 ~ +60	○	○
-20 ~ +70	○	○
-40 ~ +85	×	○

* ○ : Available △ : Conditional X : Not available

* Inclusive of calibration @ 25 °C, operating temperature range, input voltage variation, load variation, aging (1st year), shock, and vibration

Note: not all combination of options are available. Other specifications may be available upon request.

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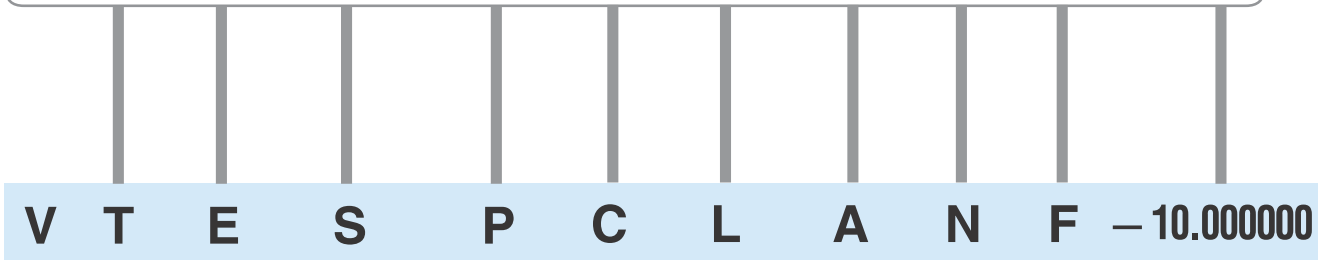
sales@taitien.com.tw

Specifications subject to change without notice.

Model Numbering Guide – VCXO

Available options

Type	package (mm)	Supply Voltage(V)	Tri-State Function	Freq.Stability/APR (ppm)	Temp. Range(°C)	Output Logic and Symmetry	Oscillator Mode	Appearance	Lead Free	Dash	Freq. (MHz)
V: VCXO	W: 5.0x3.2 (6 Pads) T: 7.0x5.0 (6 Pads) K: 14.2x9.3 (6 Pads) L: 14.0x9.0 (4 Pads)	C: 5 (Only for L Package) E: 3.3 J: 2.5 K: 1.8 (Only for CMOS and Frequency < 60MHz)	U: Relative Pulling (Refer to Center Voltage) with Tri-State to pin 2 M: Multiplier Frequency with Tri-State to pin 2 S: Enable Low R: Input to pin 5 F: Without Tri-State	M: ±25/±50 (VC=10%Vdd ~90%Vdd) P: ±50/±50 (VC=10%Vdd ~90%Vdd) A: ±50/±50 (VC=0V~Vdd) B: ±25/±50 (VC=0V~Vdd) V: Overall: ±35ppm Pulling: ±35ppm	I: -10~+60 C: -20~+70 L: -40~+85 J: -40~+105	J: CMOS 15pF / 50±5% F: CMOS 50pF / 50±5% L: LVPECL / 50±5% V: LVDS / 50±5% W: Sine Wave	A: AT Fundamental T: AT 3 rd Overtone Not selectable by Customer	N: Normal F: Option A G: Option B J: Option C	F: RoHs Compliant	-	XX.XXXXXX



*Not all combinations of options are available.

Example: VTESPCLANF-10.000000

Type	VCXO
Package	7.0 x 5.0 mm
Supply Voltage(V)	3.3 V
Tri-State	Enable Low
Freq. Stability / APR	±50ppm / ±50ppm
Temp Range	-20~+70 °C
Output	LVPECL/Symmetry 50±5%
Oscillator Mode	AT Fundamental
Appearance	Normal Appearance
Lead Free	RoHs Compliant
Frequency	10.000000 MHz